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Electrode dependent interfacial layer variation in Metal-Oxide-Semiconductor capacitor

I-S Park[1,2], Y C Jung[1], M Lee[1], S Seong[1], and J Ahn[1]
[1] Department of Materials Science & Engineering, Hanyang University, Seoul, Korea
[2] Institute of Nano Science and Technology, Hanyang University
222 Wangsimni-ro, Seongdong-gu, Seoul 133-791, Korea

E-mail: jhahn@hanyang.ac.kr

Abstract. The interfacial layer between oxide and semiconductor in metal-oxide-semiconductor (MOS) capacitors depends on the metal electrode material. The metal/HfO_2/Si and metal/HfO_2/Ge capacitor were made using an atomic layer deposited HfO_2 dielectric films and Mo, Ru, and Pt electrodes above Si substrate and Ti, Ru, and Pt electrodes above Ge substrate. The measured saturation capacitance was varied with electrode and evaluated to capacitance equivalent thickness (CET). In Si-based MOS capacitor, the CET value of the capacitor with Pt electrode is larger than those with Mo and Ru electrode. In addition, the CET is 27.4 A, 38.2 A, and 30.8 A for Ti, Ru, and Pt electrode, respectively, for Ge-based MOS capacitors. The CET variation with electrode is attributed the variation of dielectric constant of HfO_2 dielectric and the difference of interfacial layer. The CET variation is well in agreement with the interfacial layer thickness taken by a transmission electron microscopy. The thickness variation of interfacial layer results from the oxygen gettering ability of the electrode even though they are apart.

1. Introduction

Si-based metal-oxide-semiconductor (MOS) transistors have faced a challenge for continuous and exponential scaling-down of feature size. With this rapid scaling of MOS transistors, that is, the decrease of channel length and gate dielectric thickness, new materials, processes, and structures have been introduced to the IC manufacturing industry [1]. As new materials, high-mobility channels, high dielectric constant (k) gate dielectrics, and metal gate electrodes are under research and development to replace Si channel, SiO_2 dielectric, and doped-polycrystalline Si electrode, respectively. With the successful introduction of high-k and metal gate (HKMG) beyond 45 nm technology [2, 3], high mobility channels such as Ge and GaAs have been focused as a further solution for the carrier mobility enhancement in logic devices. On the high-k/semiconductor interface, the native oxide, playing a role of additional dielectric with high-k oxide, is a layer to decrease the capacitance of MOS transistor. With scaling-down of devices, the interfacial native oxide should be controlled and reduced for higher capacitance [4, 5]. When the devices are processed with the same high-k deposition and post-annealing, the capacitance of capacitor is strongly dependent on the metal electrode materials. The value of capacitance is easily compared in term of equivalent oxide thickness (EOT) or capacitance equivalent thickness (CET). The electrode dependent CET of capacitor has also been reported [6, 7].

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Atanassova *et al.* reported the EOT and dielectric constant variation of Ta_2O_5 MOS capacitors with Al, Au, W, TiN, and TiN/W electrodes, and suggested that these variations are related to the gate electrode/Ta_2O_5 interaction during electrode deposition [6]. Kim *et al.* also reported the EOT decrement of HfO_2 and ZrO_2 MOS capacitors when Ti is used as a top electrode compared to those of Al and Pt, and claimed that this decrement comes from the decomposition of the SiO_2 interfacial layer between high-k dielectric and Si substrate [7].

Atomic layer deposition (ALD) has been widely employed to making high-k gate oxides [1, 4, 5]. In ALD, the film grows through a self-limiting surface reaction between precursors that are alternately supplied into a substrate. The precursors are separated by inert gas purging to remove the physisorbed precursor and to block the gas-phase reaction between precursors. Even though the ALD method has the disadvantage of low growth rate, it offers high-quality thin films, excellent atomic-level thickness controllability and uniformity in a wide surface, high conformality, and excellent repeatability.

Metal for gate electrode applications requires a suitable work function and thermal stability [8, 9]. Single metal electrodes with a higher work function similar to conduction band such as Pt and Ru are the promising candidates for p-MOS devices and that with a lower work function similar to valence band such as Ti are for n-MOS. Mo electrode has applied for p-MOS, n-MOS and midgap devices.

In this work, the capacitance variations of both Si- and Ge-based MOS capacitors were investigated with the structures of metal/ALD-HfO2/Si and metal/ALD-HfO2/Ge using capacitance-voltage (C-V) measurements. The capacitance was dependent on a metal electrode even though the capacitors were processed indentically except for the electrode specimen. To investigate the structural status of interfacial layers concerning to this capacitance variation, cross-sectional transmission electron microscopy (TEM) analyses were also conducted.

2. Experiments

The substrates used in this study were p-type (100) Si wafers with B of 3×10^{15} atoms/cm^3 doping concentration and p-type (100) Ge wafers with Ga of 4.5×10^{17} atoms/cm^3 each other. Prior to HfO_2 deposition on Si wafers, standard RCA cleaning with final 100:1 HF-dip for 10 sec was performed to remove the native oxide and also on Ge wafers, wet chemical cleaning was performed with 100:1 HF dipping, followed by DI water rinse for five cycles [10]. High-k HfO_2 dielectric films were deposited in a travelling-wave type ALD reactor (made by CN1) using a liquid $Hf[NCH_3C_2H_5]_4$ precursor and H_2O oxidant. Hf precursor was volatilized from the canister heated at 60°C and was carried into the reaction chamber with a carrier gas of N_2. Nitrogen was also used as a purge gas. The canister containing H_2O was kept at room temperature and no carrier gas was used to deliver it to the ALD reactor due to its high vapor pressure. After HfO_2 film deposition, square-type gate pattern was defined using a conventional photolithography process. And then, top electrodes such as Mo, Ru, Pt, and Ti were deposited on HfO_2 film and photoresist by a DC magnetron sputtering system at room temperature. In case of Ti electrode, Pt was also stacked on it to prevent its surface oxidation. The base pressure of the sputter system was less than 2×10^{-6} torr and deposition was performed at 3×10^{-3} torr. The back surfaces of the substrates were metallized to provide ohmic contact to semiconductor substrate for electrical measurements. The fabricated MOS capacitors were treated by forming gas anneal (FGA) for 30 min in N_2 ambient with 5 % H_2 at 400°C.

The C-V measurements were performed in parallel mode at 1 MHz frequency using a HP4284 LCR meter by sweeping from 2 V to -2 V. For the cross-sectional analyses for the interfacial layer (IL), TEM measurements were performed for all MOS capacitors.

3. Results and Discussion

Figure 1 shows the typical C-V curves of metal/HfO_2/Si MOS capacitors with Mo, Ru, and Pt metal electrodes. The physical thickness of high-k HfO_2 on native oxide is the same 5 nm. The saturated capacitance at -2 V could be evaluated into CET for comparison and the measured CET is 19.5 A, 20.7 A, and 26.0 A for Mo, Ru, and Pt electrode, respectively. It is observed that the CET value of the capacitor with Pt electrode is larger than those with Mo and Ru electrode, even though all capacitors

were processed indentically except for the material specimen of metal electrode. Another apparent feature is the shift of C-V curves with metal electrode material. The C-V curve of capacitor with Pt electrode is much shifted positive direction with respect to those with Mo and Ru electrode. The shift of C-V curves is relatively in agreement with the work function variation of the metal materials [4].

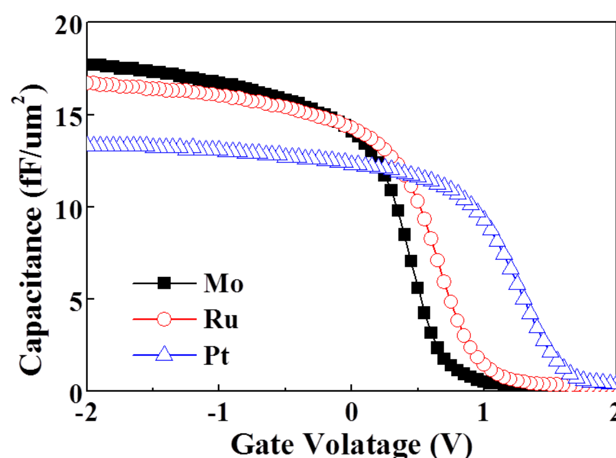

Figure 1. Electrode material dependent C-V characteristics of metal/HfO_2/Si MOS capacitors with Mo, Ru, and Pt electrode, respectively. The high-k HfO_2 films are 5 nm thick.

In addition, Fig. 2 shows the typical C-V curves of metal/HfO_2/Ge MOS capacitors with Ti, Ru, and Pt metal electrodes. These curves of Ge-based MOS capacitors are very different with those of Si-based capacitors in Fig. 1. It is found a stretch-out in the C-V curve meaning many interfacial traps and a higher value of in the inversion region indicating an additional and parasitic capacitor generated near a Ge substrate. On the parasitic capacitance at inversion region for capacitors with Ru electrode, Cmin/Cmax for Si capacitor is 1.8 % but that for Ge is 18.2 % where Cmin is the minimum capacitance and Cmax is the maximum. These results indicate the unstable GeO_x interfacial layer formation on Ge substrate. It is also observed the saturated capacitance at -2 V is dependent on the metal electrode and the measured CET is 27.4 A, 38.2 A, and 30.8 A for Ti, Ru, and Pt electrode, respectively. Interestingly, the CET value of the capacitor with Ru electrode is larger than that of Pt electrode. It is the opposite result with that for Si substrate. For the shift of C-V curves, it is very little in case of Ge substrate due to the Fermi level pinning [11].

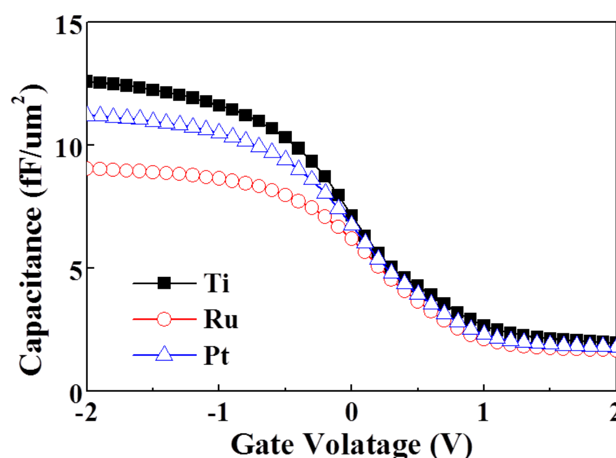

Figure 2. Electrode material dependent C-V characteristics of metal/HfO_2/Ge MOS capacitors with Ti, Ru, and Pt electrode, respectively. The high-k HfO_2 films are 5 nm thick.

As the capacitance of simple capacitor is expressed in form of C = kA/d where k is the dielectric constant of dielectric, A is the effective area of capacitor, and d is the thickness of dielectric. And, CET can be evaluated as CET = 3.9A/C_m, where k of SiO_2 is 3.9 and C_m is the measured capacitance in maximum. When three dielectrics are stacked in parallel, the total CET = CET_1 + CET_2 + CET_3, where CET_n is CET of n-th dielectric. In the MOS capacitor, usually, three dielectric layers are can be supposed, that is, 1) the bottom IL between oxide and semiconductor, 2) main dielectric (it will be denoted as dielectric), and 3) the top IL between metal and oxide.

To identify ILs and dielectric affecting to capacitance variation with metal electrode, TEM images of MOS capacitors were taken as shown in Fig. 3. It is found that the Ge surfaces under bottom IL are much rougher than Si surfaces due to the softness of Ge against wet HF chemical. At first, it is observed that top ILs show rough surface compared to bottom ILs but there is not so apparent layer in all images in Fig. 3. For the HfO_2 dielectrics, their structures were not crystallized on Si and Ge substrates due to the low thermal budget. Their values of dielectric constant on Si are 17.7, 18.8, and 23.2, respectively, which were evaluated from the relationship between EOT and the physical thickness of HfO_2 films [4]. Considering the dielectric constant of HfO_2, for example 17.7, the contribution of HfO_2 film with 4.5 A (k(HfO_2)/k(SiO_2)) corresponds to 1 A of CET. The higher the dielectric constant of HfO_2 is, the lower its contribution to CET is. This result indicates that the dielectric constant of dielectric is strongly dependent on the top metal electrode. This dependence comes from the deposition process of electrode and post-annealing [6], which attribute to the inter-diffusion of elements in both dielectric and electrode.

For the bottom ILs, they show obviously different thickness in the TEM images with electrode. In case of Si substrate, the IL with Pt electrode is about 15 A whereas those with Mo and Ru electrodes are about 7-8 A. This difference is well in agreement with the difference of CET in Fig. 1. For Ge substrate, the ILs below Ti and Pt are much thinner than IL below Ru, so that CET of the capacitors with Ti and Pt result in a lower value. Ti film as well as Ba, Ti, Zr, Hf, V, Nb, and Ta is well-known as one of oxygen-getter materials [12]. Assuming the gettering ability of Ti film whether it is apart with IL and so IL becomes thinner after electrode deposition and FGA, other metal layers such as Mo, Ru, and Pt can also getter the oxygen in ILs. However, the gettering effect is different with the specimen of bottom IL. For example, Ru film can getter the IL on Si but not much on Ge as shown in Figures. 3(b) and 3(f). It is found that Mo and Ru films are efficient at gettering oxygen from SiO_2 IL and Ti and Pt films are from GeO_x IL. In addition, the oxygen gettering of electrode from the oxide film, HfO_2, gives rise to variation of dielectric constant of dielectric film.

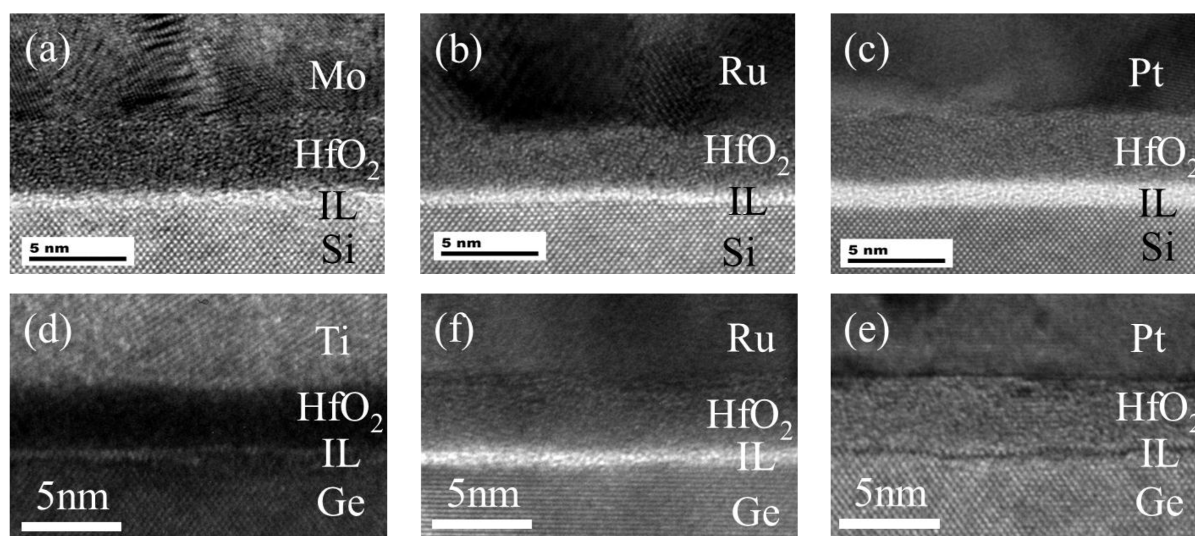

Figure 3. Cross-sectional TEM images of metal/HfO_2/Si MOS capacitors with the electrode of (a) Mo, (b) Ru, and (c) Pt and metal/HfO_2/Ge capacitors with (d) Ti, (e) Ru, and (f) Pt electrode, respectively.

4. Conclusion

The electrode dependent ILs in MOS capacitors of metal/HfO_2/Si and metal/HfO_2/Ge are investigated by using C-V measurements and cross-sectional TEM analyses. The metal/ALD-HfO_2/Si capacitors with Mo, Ru, and Pt electrode and metal/ALD-HfO_2/Ge capacitors with Ti, Ru, and Pt electrode were fabricated. The measured values of CET were varied with electrode material. In Si-based MOS capacitor, the CET value of the capacitor with Pt electrode is larger than those with Mo and Ru electrode. In addition, the CET is 27.4 A, 38.2 A, and 30.8 A for Ti, Ru, and Pt electrode, respectively, for Ge-based MOS capacitors. The CET variation is attributed to the variation of dielectric constant of HfO_2 film and the thickness difference of IL. The CET variation is well in agreement with the thickness of ILs. Even though electrode and IL are apart, the oxygen-gettering of the electrode affects to IL. The choice of electrode is a promising approach to control the state of IL on semiconductor for the higher capacitance.

Acknowledgments

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