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## Electrically Tunable and Negative Schottky Barriers in Multi-layered Graphene/MoS<sub>2</sub> Heterostructured Transistors

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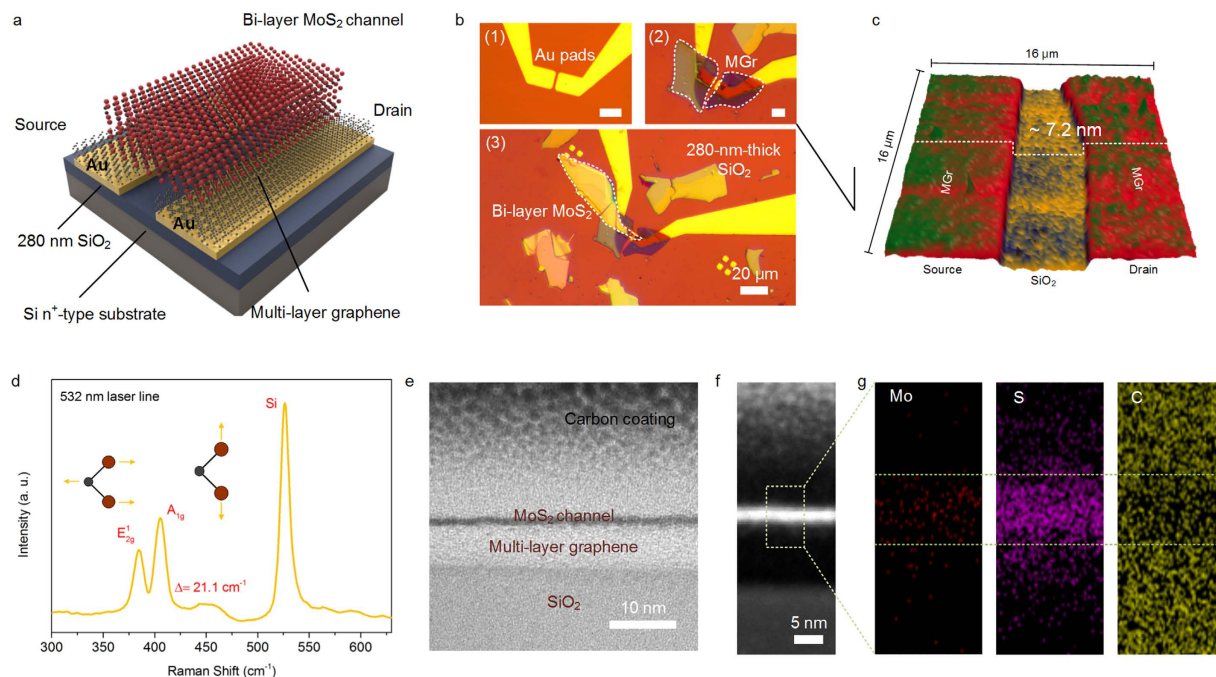
We fabricated multi-layered graphene/MoS<sub>2</sub> heterostructured devices by positioning mechanically exfoliated bulk graphite and single-crystalline 2H-MoS<sub>2</sub> onto Au metal pads on a SiO<sub>2</sub>/Si substrate via a contamination-free dry transfer technique. We also studied the electrical transport properties of Au/MoS<sub>2</sub> junction devices for systematic comparison. A previous work has demonstrated the existence of a positive Schottky barrier height (SBH) in the metal/MoS<sub>2</sub> system. However, analysis of the SBH indicates that the contacts of the multi-layered graphene/MoS<sub>2</sub> have tunable negative barriers in the range of 300 to −46 meV as a function of gate voltage. It is hypothesized that this tunable SBH is responsible for the modulation of the work function of the thick graphene in these devices. Despite the large number of graphene layers, it is possible to form ohmic contacts, which will provide new opportunities for the engineering of highly efficient contacts in flexible electronics and photonics.

### Introduction

Among layered 2-dimensional (2D) materials, molybdenum disulfide (MoS<sub>2</sub>) is attracting attention as a semiconducting material in the transition metal dichalcogenide family<sup>1,2</sup>. Because of quantum mechanical confinement, MoS<sub>2</sub> possesses several remarkable properties, such as an absence of dangling bonds<sup>3</sup>, a lack of inversion symmetry<sup>4</sup>, valley degrees of freedom<sup>5</sup>, and other fascinating physical properties; as a result, it shows promise as a novel candidate material for high-performance and low-power electronics applications<sup>6</sup>. Moreover, the individual layers, which interact through the van der Waals force, can be readily exfoliated into atomically thin layers<sup>7</sup>, and when this method is applied to combine MoS<sub>2</sub> with other 2D materials, novel heterostructured devices can be constructed<sup>8</sup>. Examples of these types of structures that have been reported in the literature include vertical tunneling transistors<sup>9,10</sup>, hybrid graphene/MoS<sub>2</sub> photoresponsive devices<sup>11</sup>, and memory devices that incorporate hexagonal boron nitride<sup>12</sup>. Although multifunctional device architectures offer various promising functionalities, various aspects of the performance-degradation effect have not been fully explored. In particular, previous studies have shown that the metal/MoS<sub>2</sub> and gate dielectric/MoS<sub>2</sub> interfaces significantly affect device performance<sup>13–15</sup>. In the case of the metal/MoS<sub>2</sub> interface, there is a scalable Schottky barrier height (SBH) that restricts carrier injection when a very low-work-function metal, such as scandium, is used<sup>13</sup>. Several previous works on contact optimization using single-layer graphene have been affected by the same difficulties<sup>16–17</sup>. However, very recently, Yu, L. *et al.*<sup>18</sup> and Liu, Y. *et al.*<sup>19</sup> have observed a barrier-free contact by using single-layer graphene as the back interconnection. Nevertheless, ohmic contact has been rarely achieved with relatively thick graphene (or graphite), and few detailed studies on the back-gate tunability of negative barrier heights have been conducted.

In this study, we present heterostructured MoS<sub>2</sub> field-effect transistors (FETs) that contain approximately 20 layers of graphene (denoted below as MGr) to form bottom-up interconnections for source

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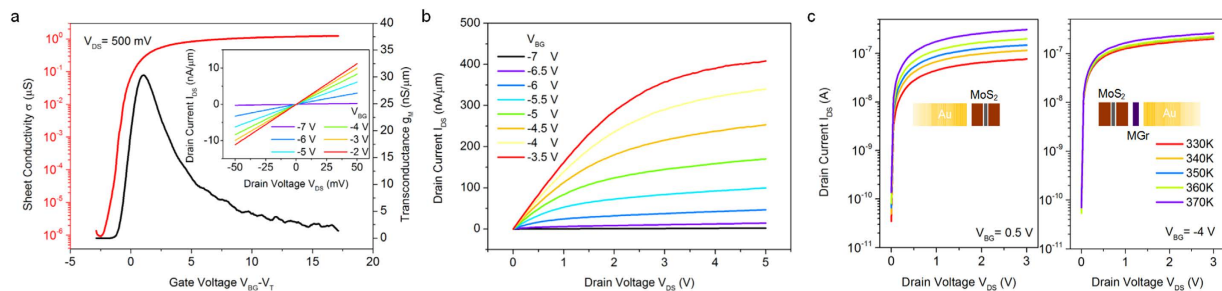


**Figure 1. Fabrication process and schematic illustration of an MGr/MoS<sub>2</sub> device.** (a) A 3D schematic image of our back-gated MoS<sub>2</sub> FET. (b) An optical image of pre-patterned Au pads (1), MGr flakes deposited on top of the Au electrodes (2), and the separation distance between them, which is defined as the channel length ( $L \sim 3.5 \mu\text{m}$ ), as well as an optical image of the transfer of MoS<sub>2</sub> flakes onto the top surface of the MGr/Au stack to form a semiconducting channel with a width of  $W \sim 5.2 \mu\text{m}$  (3). (c) 3D AFM topographic image of MGr source/drain electrodes deposited on a 280-nm-thick SiO<sub>2</sub>/Si substrate. (d) The Raman signal collected from the deposited MoS<sub>2</sub> channel in the MGr/MoS<sub>2</sub> FET and compared with that of MoS<sub>2</sub> flakes, as shown in Figure S2. (e) Cross-sectional HRTEM image of the heterostructured FET. (f) STEM image showing the interface between the MGr and the few-layered MoS<sub>2</sub> as well as the top of the carbon-Pt coating. (g) EDX mapping of the selected area for the Mo, S, and C elements.

and drain electrodes. Here, an alternative approach was engineered by inserting a thick graphene layer instead of single-layer graphene. To compare the characteristics of the devices, reference samples without MGr contacts were also fabricated. The heterostructured FETs exhibited a dramatic reduction in SBH based on the framework of the thermionic emission theory. It appeared that the observed negative SBH gave rise to true ohmic contact.

## Results

**Fabrication of the devices.** A 3-dimensional (3D) schematic representation of our heterostructured device architecture is depicted in Fig. 1a. To investigate the electronic properties of the back-gated MGr/MoS<sub>2</sub> heterostructured devices, we deposited mechanically exfoliated graphite and single-crystalline 2H-MoS<sub>2</sub> onto a SiO<sub>2</sub>/Si substrate on which Au metal pads (110 nm thick) had been pre-patterned, as described in the Methods section. The dry transfer technique used for both 2D materials began with the introduction of an intermediate polydimethylsiloxane (PDMS) layer, which acted as a contamination-free viscoelastic material to avoid wet chemistry (more information can be found in the Supplementary Information, Figure S1). Two multi-layered graphene samples were transferred from the PDMS layer to serve as the source and drain, as shown in Fig. 1b. Subsequently, a MoS<sub>2</sub> flake was directly transferred on top of the graphene flakes, overlapping both graphene contacts, to form a semiconducting channel using the same method (see (3) in Fig. 1b). For comparison, we also fabricated un-encapsulated bi- to quad-layer MoS<sub>2</sub> FETs (denoted below as Au/MoS<sub>2</sub>) without inserting an MGr layer; for these devices, the transfer procedure was reduced to only one step. The MoS<sub>2</sub> channel was verified using Raman spectroscopy and atomic force microscopy (AFM) to confirm the thickness of the MoS<sub>2</sub> flakes (see Fig. 1d and the Supplementary Information, Figures S2 and S3). The frequency difference of  $21.1 \text{ cm}^{-1}$  between the in-plane mode ( $E_{2g}^1$ ) and the out-of-plane mode ( $A_{1g}$ ) corresponds to the signal of bi-layer MoS<sub>2</sub>, which is consistent with our MoS<sub>2</sub> reference sample (Figure S2) and other reports<sup>20</sup>. Optical microscopy and AFM were used to determine the MGr thicknesses, which were 7.1 and 7.3 nm for the source and drain, respectively, as shown in Fig. 1c. The average height of the graphene flakes was further characterized using statistical studies and was found to be  $\sim 7 \text{ nm}$  (Figure S4). Cross-sectional high-resolution



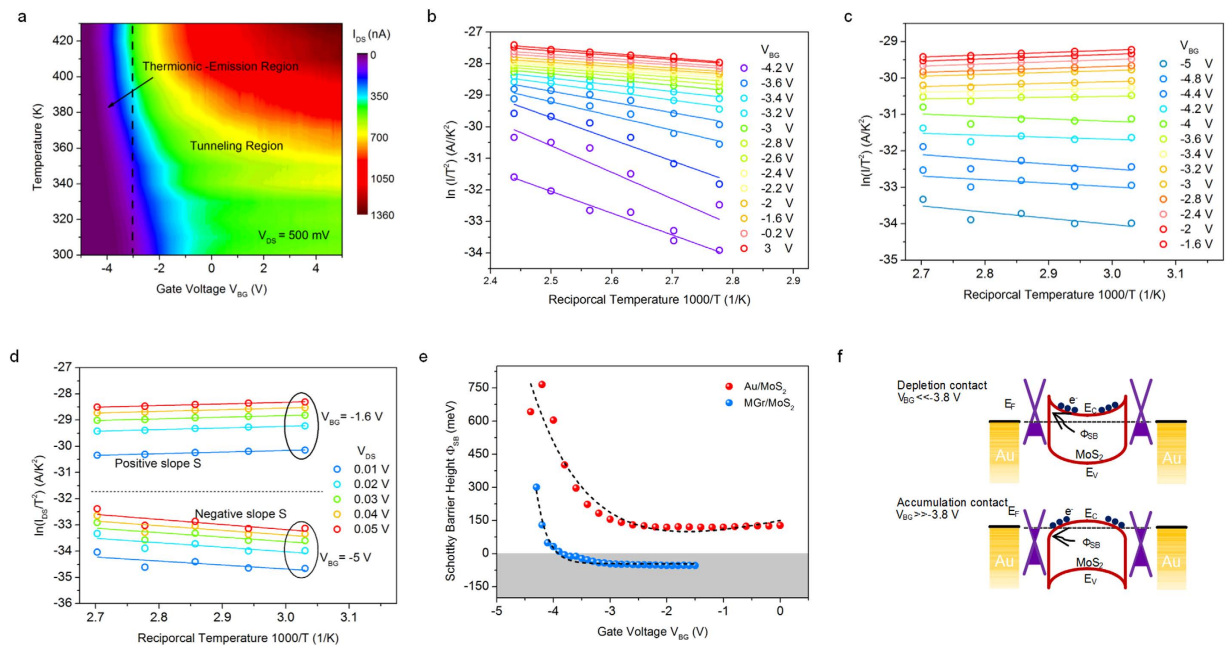
**Figure 2. Electrical performance of the transistors.** (a) Normalized I-V transfer characteristics of a typical back-gated MGr/MoS<sub>2</sub> device at a fixed drain voltage. Inset: I<sub>DS</sub>-V<sub>DS</sub> curve at a low drain bias ( $V = \pm 50$  mV). The linearity was maintained under various gate voltages. (b) Output characteristics at various gate voltages. (c) Left: Temperature-dependent (from 330 to 370 K in 10-K increments) I<sub>DS</sub>-V<sub>DS</sub> characteristics for an Au/MoS<sub>2</sub> FET (left) and an MGr/MoS<sub>2</sub> FET (right). The inset shows the corresponding device configurations.

transmission electron microscope (HRTEM) analysis was used to study the overlapped MGr/MoS<sub>2</sub> stack. An HRTEM image of a clear and compact interface, without other impurities or significant gaps between the MoS<sub>2</sub> and MGr, is shown in Fig. 1e. Figure 1f displays a scanning TEM (STEM) image of the MGr/MoS<sub>2</sub> heterostructure, and the corresponding energy-dispersive X-ray spectroscopy (EDX) mapping is shown in Fig. 1g and S5.

**Characterization of the devices.** To investigate the presence of the intermediate MGr layer in our MGr/MoS<sub>2</sub> devices and its influence on the Schottky barrier, the devices were electrically characterized at room temperature. Figure 2a shows the typical I<sub>DS</sub>-V<sub>BG</sub> transfer characteristics of the back-gated heterostructured FETs, which are presented as a normalized sheet conductivity (defined as  $\sigma = I_{DS}/V_{DS}(L/W)$ ) as a function of  $V_{BG} - V_T$  where  $V_{BG}$  is the gate voltage and  $V_T$  is the threshold voltage. The devices displayed obvious n-type behavior and produced a high on/off ratio ( $\sim 10^6$ ) with a maximum normalized transconductance  $g_M/W$  of approximately 30.4 nS/ $\mu$ m at  $V_{DS} = 500$  mV. I-V hysteresis behavior is also shown in Figure S6. After *in situ* thermal heating, the devices exhibited nearly “hysteresis-free” behavior, indicating that the amount of adsorbates was negligible<sup>21</sup>. By contrast, the devices without an MGr layer demonstrated a transconductance of 0.35 nS/ $\mu$ m at  $V_{DS} = 500$  mV, which is 2 orders of magnitude lower than that of the MGr/MoS<sub>2</sub> FETs, as shown in Figure S7. The field-effect mobility,  $\mu_{FE}$ , was estimated from the maximum value of the transconductance using the expression  $\mu_{FE} = g_M L / W C_{OX} V_{DS}$ . Here,  $C_{OX} = \epsilon_r \epsilon_0 / d_{OX} \sim 1.23 \times 10^{-8}$  F/cm<sup>2</sup> ( $\epsilon_0 = 8.854 \times 10^{-14}$  F/m,  $d_{OX} = 280$  nm), which is the back-gate capacitance per unit area, and  $g_M = dI_{DS}/dV_{BG}$  is the transconductance. Thus, the field-effect mobility for our bi-layer MGr/MoS<sub>2</sub> device appeared to be approximately 17.9 cm<sup>2</sup>/Vs in the bi-layer MoS<sub>2</sub> channel, as presented in Figure S8. This measured mobility is comparable to those of mono- or bi-layer MoS<sub>2</sub> in high- $\kappa$  gate dielectric capping devices<sup>22,23</sup>. The reference sample (thick bi-layer MoS<sub>2</sub>) with an Au metal contact had a mobility of 0.2 cm<sup>2</sup>/Vs, which is consistent with other reports<sup>3,24,25</sup>. Such a low mobility may be originated from the presence of a sizable Schottky barrier at the Au-MoS<sub>2</sub> interface that hinders efficient carrier injection. To extract an accurate gate capacitance for the mobility calculation, a 100-kHz capacitance-voltage (C-V) profile was obtained by measuring between the source and back-gate electrodes (see Figure S9). The floor value of the capacitance (the minimum capacitance in the inversion regime) represented the actual electrode capacitance<sup>26</sup>, and the measured gate capacitance ( $\sim 1.24 \times 10^{-8}$  F/cm<sup>2</sup>) was very close to the value of  $1.23 \times 10^{-8}$  F/cm<sup>2</sup> obtained in the above calculation for a 4.52-mm<sup>2</sup> contact area.

**Extraction of the Schottky barrier height.** Figure 2b displays the I<sub>DS</sub>-V<sub>DS</sub> output characteristics of the MGr/MoS<sub>2</sub> devices at various gate voltages. The saturation current could be reached at high drain voltages under certain gate biases, opening a wide drain voltage window. Moreover, the drain current, I<sub>DS</sub>, exhibited symmetrical and linear behavior (inset of Fig. 2a) under a small source-drain bias sweep ( $\pm 50$  mV). Previous studies have claimed that the linear relationship in the range of low V<sub>DS</sub> bias suggests ohmic contact at the metal-to-semiconductor junction<sup>27</sup>. However, the present experimental findings imply the existence of a sizable energy barrier at the two back Schottky diodes based on detailed variable-temperature measurements. Remarkably, the I<sub>DS</sub>-V<sub>DS</sub> characteristics at a fixed gate bias, on the right-hand side of Fig. 2c, manifested an extremely weak temperature dependence in the temperature range from 330 to 370 K compared with the Au/MoS<sub>2</sub> sample (left-hand side of Fig. 2c). This weak temperature dependence implies a reduction in the barrier height for thermal emission due to the modification of the barrier at the MGr/MoS<sub>2</sub> interface.

To better understand how the carriers travel in the presence of a Schottky barrier, we employed a well-known model, *i.e.*, the 3D thermionic-emission theory, to describe our observations. Generally, the two carrier transport mechanisms are thermionic emission and quantum-mechanical tunneling under



**Figure 3. Temperature dependence of electrical transport and the extraction of the Schottky barrier height.** (a) Color map of the temperature-dependent transfer characteristics at  $V_{DS} = 500$  mV. (b,c) Arrhenius plots of  $\ln(I_{DS}/T^2)$  vs.  $1000/T$  at various gate voltages for an Au/MoS<sub>2</sub> FET (b) and an MGr/MoS<sub>2</sub> FET (c). (d) Arrhenius plot for  $V_{BG} = -1.6$  V and  $-5$  V at various drain voltages from 10 to 50 mV. (e) Gate bias dependence of the variations in the Schottky barrier height. (f) Top: Schematic band diagram for a depletion-type contact. Bottom: Illustration of an accumulation contact.

gate bias modulations, as shown in Fig. 3a. The former current mechanism is associated with the emission of majority carriers over the interfacial barrier, and the tunneling mechanism involves carriers crossing the barrier in a highly accumulated MoS<sub>2</sub> channel. Under the assumption that the current is predominantly governed by the thermionic emission theory, the current  $I_{DS}$  is given by the expression<sup>28</sup>  $I_{DS} = AA^*T^2 \exp(-e\Phi_{SB}/k_B T) [\exp(eV_{DS}/k_B T) - 1]$ , where  $A^*$ ,  $A$ ,  $e$ ,  $V_{DS}$ , and  $k_B$  are the Richardson constant, the area of the contact, the elemental charge, the drain voltage, and the Boltzmann constant, respectively. Temperature-dependent I-V data were collected in the high-temperature regime (above room temperature) to avoid weak conductivity variations (see the Supporting Information, Figure S10). Such variations occur because at low temperature in the off state, the carriers do not have sufficient energy to pass through the barrier, and thermionic emission theory fails to explain this behavior (a detailed discussion can be found in ref. 29). To determine the SBH, the reciprocal temperature dependence of the  $\ln(I_{DS}/T^2)$  fit curve was plotted for various gate voltages at the Au/MoS<sub>2</sub> (Fig. 3b) and MGr/MoS<sub>2</sub> (Fig. 3c) interfaces. The slope,  $S$ , was extracted from the different  $V_{BG}$  values of the Arrhenius plot, and the intercept,  $S_{INT}$ , yielded the Schottky barrier height,  $\Phi_{SB}$ , as a function of the gate voltage,  $V_{BG}$ , using the expression  $S_{INT} = -e\Phi_{SB}/1000k_B$  (see the Supporting Information, Figure S11). For the MGr/MoS<sub>2</sub> devices, the slope of the linear fit curve in the Arrhenius plot is negative near the off state (low  $V_{BG}$ ;  $-5$  V) and becomes more positive with the formation of a highly conductive MoS<sub>2</sub> channel at  $V_{BG} = -1.6$  V, as depicted in Fig. 3d. The resulting features imply that the SBH dramatically decreases from 300 to 0 meV, becomes negative, and finally saturates near  $-45.5$  meV, as shown in Fig. 3e. This finding represents the first observation of negative SBH behavior at an MGr/MoS<sub>2</sub> contact and is contrary to the results of several studies that have investigated this phenomenon in the 0–300 meV range<sup>16–19</sup>. Similar findings have been reported in conventional semiconductors and novel 2D materials, *e.g.*, MoS<sub>2</sub> with ferromagnetic permalloy contacts<sup>29</sup>, p-type MoS<sub>2</sub> with MoO<sub>x</sub><sup>30</sup>, and silicon (001) with metal Ti<sup>31</sup>. By contrast, for the Au/MoS<sub>2</sub> contact considered in this study, under a negative gate bias, the current through the Schottky barrier *via* thermionic emission resulted in a linearly decreasing trend (from 765.9 to 118.8 meV) as the gate bias became forward directed.

**Negative Schottky barrier behavior.** Generally, the semiconductor surface states and the work functions of the metal play a decisive role in the determination of the SBH, but the details of Schottky barrier formation in metal/semiconductor systems are not well understood. Various previous studies on metal/MoS<sub>2</sub> contacts have demonstrated an independence of the metal work functions due to the presence of interfacial states,  $D_{IT}$ , that cause Fermi-level pinning<sup>13,14,32,33</sup>. By combining the experimental

data presented in Figure S12 of the Supporting Information, we estimated  $D_{IT}$  using the expression<sup>28</sup>  $D_{IT} \approx 1.1 \times 10^{13}(1 - S_0)/S_0 \approx 7.9 \times 10^{13}$  states/eV cm<sup>2</sup>, where the slope is  $S_0 = d\Phi_{SB}/d\Phi_M \approx 0.12$  and  $\Phi_M$  is the metal work function. However, when MGr and MoS<sub>2</sub> are brought into contact, the Schottky-Mott model does not hold, because  $D_{IT} \neq 0$ . A modified model can be written as follows<sup>34</sup>:

$$\Phi_{SB} = S_0(\Phi_{MGr} - e\chi) + (1 - S_0)(E_G - \Phi_N) \quad (1)$$

where  $\Phi_{MGr} = 4.5$  eV and  $\chi = 4.0$  eV are the work function of the graphene and the electron affinity of the MoS<sub>2</sub><sup>35,36</sup>, respectively;  $E_G = 1.6$  eV is the band gap of the bi-layer MoS<sub>2</sub>; and  $\Phi_N = 1.53$  eV is the neutral level of the interface states. In practice, the Fermi level is pinned at a certain energy, and then, a depletion contact with a positive Schottky barrier is created at the MGr/MoS<sub>2</sub> interface. Considering this behavior, the first term of equation (1) will change to a negative value under the influence of the gate voltage, forming an accumulation contact (with a negative barrier height), at which the preferred ohmic contact can be formed (as shown in Fig. 3f). Because  $\Phi_{MGr}$  depends on the back-gate electric field, the carrier density in the MGr shifts the Fermi level by  $\Delta E_{F,MGr} = \hbar v_F \sqrt{\nu_T} |C_{OX}/e(V_{BG} - V_T)|$ , where  $\nu_F$  is the Fermi velocity. The tunability of the work function of graphene has been demonstrated by Yu, Y.-J. *et al.*<sup>37</sup> only for the single- and bi-layer cases, not for thick layers such as those used in our experiments. Furthermore, if the work function of the multi-layered graphene,  $\Phi_{MGr}$ , is less than that of the MoS<sub>2</sub>, *i.e.*,  $\Phi_B(V_{BG}) = \Phi_{MGr} - \Phi_{MoS_2}(V_{BG})$ , then it is possible for a negative contact potential,  $\Phi_B(V_{BG})$ , to arise as shown in Fig. 3f. As demonstrated by Li, Y. *et al.*<sup>38</sup>, the electric-field-driven modulation of the work function of MoS<sub>2</sub> is estimated to be  $\Phi_{MoS_2}(V_{BG}) = e(\chi + \phi_S) - \hbar\pi(C_{OX}/e)(V_{BG} - V_T)/2m^*$ , where  $\phi_S$ ,  $\hbar$ , and  $m^*$  are the surface potential, Planck's constant, and the effective mass of bi-layer MoS<sub>2</sub>, respectively. For the values given in ref. 38, the Fermi-level variation,  $\Delta E_{F,MoS_2}$ , of the bi-layer at the turning point voltage ( $V_{BG} = -3.8$  V) is only approximately 31 meV, which is quite small. Therefore, we suggest that the tunable Schottky barrier is primarily responsible for the modulation of the work function of the thick graphene. Despite the large number of graphene layers, ohmic contacts can be formed, which will provide new opportunities for the engineering of highly efficient contacts in flexible electronics and photonics applications.

## Discussion

In summary, we fabricated heterostructured MoS<sub>2</sub> FETs with multi-layered graphene contacts and systematically investigated their electronic properties at the MGr/MoS<sub>2</sub> interface. Negligible hysteresis was observed because of the optimized fabrication procedure. Upon the insertion of an intermediate tunnel layer, the devices displayed highly improved performance in terms of carrier mobility. An interesting negative Schottky barrier behavior was observed between the MoS<sub>2</sub> and the multi-layered graphene. We also qualitatively discussed the formation of ohmic contacts, which likely contributed to the controllability of the graphene work function by gate bias modulation. Thus, we were able to improve the carrier injection behavior and reduce the contact resistance, thereby developing a new possible approach for future electronics applications.

## Methods

Multi-layered graphene was mechanically exfoliated from single-crystalline graphite (from Graphene Supermarket) using the standard Scotch-tape-based cleavage method. The thick graphene flakes were transferred onto bottom gold electrodes, which served as the source and drain, using techniques described previously<sup>39</sup>. In brief, this technique was based on the use of a viscoelastic PDMS layer that served as an acceptor surface in place of a silicon substrate. The 2D flakes were deposited on the PDMS layer and then aligned on top of the Au pads using optical microscopy. We then brought the 2D/PDMS stack into contact with the target substrate and slowly peeled it away from the PDMS.

Before the dry transfer was performed, the gold electrodes were pre-patterned on a degenerately doped Si substrate covered with a 280-nm layer of SiO<sub>2</sub>. We intentionally chose two similar thicknesses of graphene flakes to perform the above techniques twice. Subsequently, MoS<sub>2</sub> (2D semiconductor) flakes were precisely deposited on top of the graphene contacts to serve as a channel material. The fabrication process described above avoids the use of any chemical solutions to minimize contamination. The devices were subsequently annealed at 399 K for 12 hours in a cryostat (ASK, 700 K) at a base pressure of  $\sim 2 \times 10^{-2}$  Torr for the removal of adsorbates. Electrical measurements were performed using a semiconductor parameter analyzer (HP, 4156A) after *in situ* vacuum annealing. C-V measurements were performed using a Precision LCR meter (Agilent, E4980A) with the samples in the same chamber.

A focused ion beam (FEI, Quanta 3D FEG) was employed to prepare cross-sectional TEM samples after the deposition of a carbon/Pt coating. HRTEM imaging was performed using a spherical-aberration-corrected TEM (JEOL, JEM-2100F) operating at 200 kV. Chemical composition mapping was performed with an EDX apparatus attached to the TEM instrument.

The numbers of layers of graphene and MoS<sub>2</sub> were determined based on the color contrast in the optical microscope images and were further confirmed by AFM (Park Systems, XE-100). Raman spectroscopy (Jaco, NRS-3100) with laser excitation at  $\lambda = 532$  nm was employed to analyze the spectra of the MoS<sub>2</sub> reference flakes and the FET channels.

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## Acknowledgments

This work was supported in part by a National Research Foundation of Korea (NRF) grant funded by the Korean government (MSIP) (NRF-2013R1A2A2A01015824).

## Author Contributions

E.K.K. proposed the research and supervised the overall study. D.Q. designed the experiment and performed the device fabrication, characterization, and data analysis. D.Q. and E.K.K. analyzed the results and wrote the manuscript.

## Additional Information

**Supplementary information** accompanies this paper at <http://www.nature.com/srep>

**Competing financial interests:** The authors declare no competing financial interests.

**How to cite this article:** Qiu, D. and Kim, E. K. Electrically Tunable and Negative Schottky Barriers in Multi-layered Graphene/MoS<sub>2</sub> Heterostructured Transistors. *Sci. Rep.* **5**, 13743; doi: 10.1038/srep13743 (2015).



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