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RESEARCH ARTICLE

An Automated Design Methodology for Ring Voltage-Controlled Oscillators in Nanometer CMOS Technologies

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ABSTRACT This paper presents a design automation methodology for ring voltage-controlled oscillators (RVCOs) with their realistic and physical characteristics captured. With multiple sets of input constraints such as target frequency, phase noise, and control voltage range, the proposed algorithm automatically finds the design candidates that satisfy the target constraints, by running iterative post-layout simulations with auto-generated layouts and testbenches. The number of post-layout simulations is significantly reduced by the backtracking algorithm that observes the simulation results and determines the search direction. The proposed algorithm is applied to generate RVCOs in 40-nm planar and 7-nm FinFET technologies for DDR5 applications, and it turns out the proposed methodology produces sets of design parameters that meet the target specification in multiple technologies.

INDEX TERMS Ring oscillators, design automation, layout generation, CMOS, FinFET, frequency control, phase noise.

I. INTRODUCTION

Various clock generation circuits have been widely used to provide synchronization signals for modern computing and communication systems. For example, transceiver circuits for process-memory interfaces require voltage-controlled oscillators (VCOs) to produce high-frequency (>10 GHz) and low-jitter (several ps-RMS) clocks to transmit and receive data symbols at high rates. Typically, two types of oscillators have been used for the clock generation purpose: *LC* and ring oscillators. *LC* oscillators utilize the resonance of *LC* tanks to generate clock signals and generally exhibit superior noise performances. Ring oscillators (Fig. 1) are typically composed of delay stages in a loop (such as CMOS inverters) and tend to occupy compact areas. They are capable of generating multiple phases as well, which makes them feasible for system-on-a-chip (SoC) applications where area consumption should be minimized and multi-phased clocks are used for their I/O interfaces [1], [2].

However, several design difficulties are associated with the design of high-quality ring oscillators. First, various design parameters are involved in implementing ring oscillators

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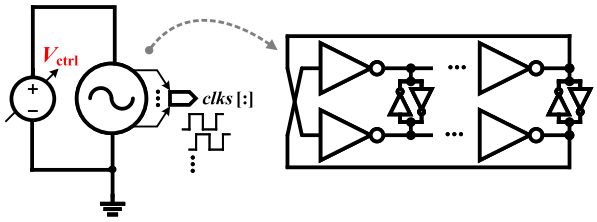


FIGURE 1. Structure of a typical ring oscillator.

that achieve desired performances, which complicates the design process significantly. For example, the oscillation frequency of a ring oscillator is affected by multiple variables such as process parameters, number of stages, transistor sizes, and supply (or control) voltage levels, in non-linear ways. Therefore, establishing an empirical and analytic relationship between those design parameters is intractable. To make matters worse, designing ring oscillators requires time-consuming transient simulations to extract time-domain metrics such as operating frequency and RMS jitter, unlike typical small-signal analog circuits such as amplifiers [3]. In addition to that, the behaviors of the ring oscillators are heavily affected by the layout-dependent effects such as parasitic capacitance, which cause more than 30 % deviations between pre-layout and post-layout characteristics in recent CMOS technology nodes such as FinFET. However, it takes significant time and effort to construct the physical layout of a ring oscillator due to the increased complexity of device structures and design rules [4], [5].

There have been several attempts to reduce the design time and overheads related to RVCO/analog circuit designs. [6] utilizes a reinforcement-learning technique with layout generators to find out the sizing parameters of analog circuits. Reference [7] trains a neural network model to automate the circuit sizing process without running SPICE simulations after the training step. Both approaches capture the layout-dependent effects by applying transfer learning techniques. However, the machine-learning-based approaches require multi-disciplinary knowledge (model selection, hyperparameter tuning, circuit design, and so on), and additional time and effort for training the neural network. References [8], [9] apply optimization techniques to design RVCO schematics with a fixed number of stages. Reference [5] utilizes digital place-and-route (PNR) techniques to produce various analog circuits including RVCO, assuming that the circuit sizing parameters are predetermined. In summary, additional research efforts have to be spent on implementing a resource-efficient RVCO design algorithm that supports automated circuit sizing and extensive parameterizations with layout effects captured.

To develop a practical circuit design technique for RVCOs that fulfills the aforementioned requirements, we propose an automated RVCO design methodology based on the research-efficient, simulation-based search algorithm with circuit schematic and "*layout*" generators. The proposed search algorithm receives various constraints such as oscillation frequency, phase noise, and control voltage range, then automatically finds the optimal set of design parameters with the minimum power consumption by running iterative post-layout simulations over design candidates. For the post-layout validations to capture layout-dependent effects, sized schematic and layout are generated by utilizing circuit design automation frameworks [10], [11] for the end-to-end automatic execution with parasitic effects captured. The number of iterative simulations associated with the searching process is reduced by a dedicated backtracking algorithm that continually narrows down the search space by utilizing the fundamental characteristics of RVCO, which is detailed in Section III. The RVCO structure with controlled supply voltage (Fig. 1) is used for the evaluation of the proposed algorithm, as the topology is widely used in typical clocking systems [2], [12], [13], though it should be noted that the proposed technique can be extended to other RVCO control methods as well [1], [14], [15], [16], [17]. Prototype RVCOs with completed layouts are generated and characterized based on the proposed method, meeting the target specifications in 40-nm planar and 7-nm FinFET technologies.

Our contributions in this work are summarized as follows:

1) An automated design method for RVCOs is presented, which captures their transient and phase-noise characteristics accurately without requiring interdisciplinary knowledge such as machine learning and/or optimization.
2) Iteration-efficient searching methods are proposed to minimize the number of post-layout simulations and converge to the optimal design point quickly.
3) The proposed search algorithm is combined with circuit generation frameworks to consider layout-dependent effects and achieve process portability in advanced CMOS technology nodes.

The reminder of this paper is structured as follows: Section II summarizes major considerations for RVCO design and automation. Section III describes the proposed design automation method for RVCOs. Finally, Section IV presents RVCO generation examples for DDR5 application from the proposed method.

II. MAJOR CONSIDERATIONS FOR RVCO DESIGN AND AUTOMATION

A. OSCILLATION CONDITION

To sustain the oscillation of an RVCO, its open-loop transfer function must meet the following Barkhausen criteria:

$$\begin{aligned} |H(j\omega_0)| &\geq 1 \\ \angle H(j\omega_0) &= 2\pi. \end{aligned} \tag{1}$$

Here, ω_0 indicates the angular frequency of the oscillator when the loop is completely closed and the conditions in (1) are satisfied. While the odd number of stage configurations always satisfies the oscillation condition [18], for an even number of stages, the loop establishes positive feedback rather than a negative one, which may result in latch-up [19].

Cross-coupled (and properly sized) latches can be attached between differential nodes to prevent latch-up as shown in Fig. 1, provoking the signal and meeting the oscillation condition by providing enough phase shift at the expense of reduced oscillation frequency. Therefore, the strength ratio between the original delay element and the latch should be carefully selected based on post-layout evaluations. Additional complexity is involved if the number of stages needs to be determined as well, for further design optimization.

B. OSCILLATION FREQUENCY

The oscillation frequency of the ring oscillator in Fig. 1 is expressed as the following expression:

$$f_{\text{osc}} \approx \frac{1}{2N \cdot (1 + k \cdot a) \cdot t_{\text{pd}}}, \tag{2}$$

where t_{pd} is the propagation delay of the core inverter that forms the loop, N is the number of stages, and k is the coefficient to represent the first-order sensitivity in t_{pd} due to cross-coupled latches. a is the latch ratio coefficient, which is defined as the width ratio of the core inverter and latch.

Assuming the relative strength of PMOS and NMOS are balanced, t_{pd} could be also approximated by the following expression [20]:

$$t_{\text{pd}} \approx \frac{L_{\text{core}} C_{\text{L}} V_{\text{ctrl}}}{W_{\text{core}} \mu C_{\text{ox}} \cdot (V_{\text{ctrl}} - V_{\text{th}})^2}, \tag{3}$$

where W_{core} and L_{core} are the channel width and length of the devices composing the core inverter, μ is the carrier mobility, V_{th} is the threshold voltage, C_{ox} is the gate-oxide capacitance per unit area, V_{ctrl} is the controlled supply voltage applied to the ring oscillator, and C_{L} is the loading capacitance, composed of the input capacitance ($C_{\text{core}} = C_{\text{ox}} \cdot W_{\text{core}} \cdot L_{\text{core}}$) and capacitance associated other components (C_{other}) such as latches and buffers. Then since $C_{\text{L}} = C_{\text{core}} + C_{\text{other}}$, we can rewrite the expression (3) as follows:

$$t_{\text{pd}} \approx \frac{L_{\text{core}} V_{\text{ctrl}} \cdot (C_{\text{ox}} L_{\text{core}} + C_{\text{other}}/W_{\text{core}})}{\mu C_{\text{ox}} \cdot (V_{\text{ctrl}} - V_{\text{th}})^2}, \tag{4}$$

then combining (2) and (4) yields the following expression for the oscillation frequency:

$$f_{\text{osc}} \approx \frac{\mu C_{\text{ox}} \cdot (V_{\text{ctrl}} - V_{\text{th}})^2}{2NL_{\text{core}} V_{\text{ctrl}} \cdot (1 + k \cdot a) \cdot (C_{\text{ox}} L_{\text{core}} + C_{\text{other}}/W_{\text{core}})}. \tag{5}$$

Equation (5) reveals that f_{osc} is determined by various factors, such as technology parameters, device-width and length, the voltage across the oscillator, and capacitance components, which complicates the design process significantly. Multiple solutions might exist for the same value of f_{osc} and designers need to choose between candidates to find out the optimal design parameters, which requires extensive design space explorations with post-layout parameters captured. Fig. 2 illustrates one example scenario that two designs with different numbers of stages (3 versus 2) and latch ratios (0.25 versus 0.875) achieve the same oscillation frequency (20 GHz). Finding out these two candidates require two-dimensional, post-layout explorations with respect to the number of stages and latch ratio, which is intractable in manual design methods. To make matters worse, various large-signal characteristics and voltage-dependent capacitances deviate the oscillation frequency from the expression (5), which increases design complexity even further.

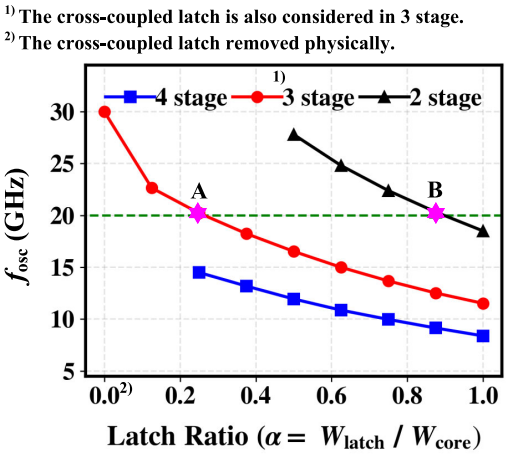


FIGURE 2. Frequency versus latch ratio (α) for different stage configurations in a 40-nm technology.

C. PHASE NOISE

The phase noise represents the fidelity of clock signals in the frequency domain in the presence of noise and disturbances. From [19], the phase noise of inverter-based ring oscillators affected by transistor thermal noise can be expressed as:

$$\mathcal{L}(\Delta f) = \frac{f_{\text{osc}}^2}{\Delta f^2} \cdot \frac{4kT\gamma}{I_{\text{d}}(V_{\text{ctrl}} - V_{\text{th}})}, \tag{6}$$

where k, T, and γ denote Boltzmann's constant, the absolute temperature, and the excess noise factor for the device's thermal noise, respectively. Δf is the frequency offset and I_{d} is the device drain current. Equation (6) indicates that the phase noise is inversely proportional to current and voltage when the oscillation frequency is fixed. In other words, increasing power consumption brings the improvement of the phase noise [19], [21], [22]. However, as the design parameters associated with the phase noise expression in (6) are coupled to the oscillation frequency as well, as expressed in (5), simply increasing power consumption to improve the phase noise characteristics may deviate the operating frequency from the original point. Therefore, additional fine-tuning processes are involved in preserving the oscillation frequency, which take a significant amount of effort in manual design approaches.

III. DESIGN METHODOLOGY FOR AUTOMATED RVCO GENERATION

As discussed in the previous section, the oscillation frequency and phase noise characteristics are affected by multiple design factors and layout effects, which results in layout

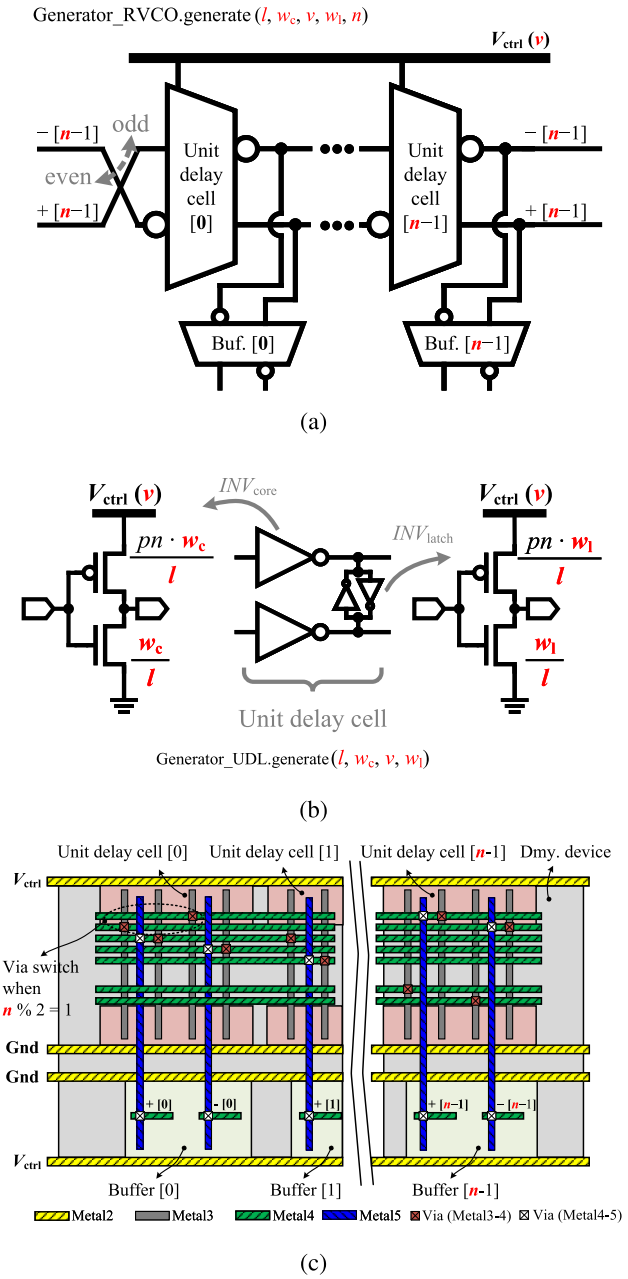


FIGURE 3. RVCO generation example (a) schematic (only two delay/buffer stages are shown) (b) unit cell schematic (c) layout.

iterations and/or sub-optimal designs. The methodology suggested in this section automatically discovers candidates that meet the target constraints (target frequency, phase noise, and control voltage range) and their layouts with reduced design efforts and iterations. Detailed explanations are provided in the following subsections.

A. AUTOMATED RVCO SCHEMATIC & LAYOUT GENERATION

In order to implement an automated sizing algorithm for RVCOs, their design entities (such as schematic, layout, and testbenches) for specific design parameters should be generated automatically. Therefore, we utilize an automatic circuit generation framework [10] and its associated layout generation engine [11]. They are used to describe the circuit generators for RVCOs that receive design parameters (i.e. the transistor width of core inverters) and produce the schematic and layout of the RVCO, and their associated testbenches to measure the frequency, power consumption, and phase noise for target operating conditions. The conceptual diagrams of the generated schematic and layout of RVCO are illustrated in Fig. 3 (only two delay/buffer stages are displayed for simplicity). The unit delay cell is composed of four CMOS inverters, two for the forwarding delay elements (or core inverters, INV_{core}) and two for the latching elements (or latch inverters, INV_{latch}). The sizing parameters for INV_{core} and INV_{latch} are chosen independently. The supply voltage of the inverters is connected to the control voltage of the RVCO, V_{ctrl} to set the propagation delay and thereby the oscillation frequency. The buffer circuits are generated and considered together with the delay cells, as their input loadings affect the oscillation frequency as well. The layout of integrated delay/buffer stages is depicted in Fig. 3(c). The layout shares the same sizing parameters with the schematic, and its differential wiring patterns are matched across entire stages, to suppress any systematic phase mismatches. The effective width and length are configured by setting the fingers and vertical stacks of transistors, to make the proposed design method feasible for advanced technologies [4], [5].

Regarding the RVCO design, we have five design parameters to be configured: the length of transistors (l), the width of core inverters (w_{c}), the width of latch inverters (w_{l}), the control voltage (v), and the number of delay stages (n)). These five variables form a 5-dimensional search space $X := \{x = (l, w_{\text{c}}, w_{\text{l}}, n, v)\}$. Note that there is a significant number of design points to be checked when the entire design points are scanned for each case (N^5 when each design parameter has N possible values). Therefore, an efficient way of searching the design space with a minimal number of observations is essential to design the RVCO within a reasonable time period.

B. CORE ALGORITHM

1) PROBLEM DESCRIPTION

The main goal of the proposed algorithm is formulated in (7). As illustrated in the formulation, the algorithm searches available design spaces and finds a set of candidates that meets key constraints such as oscillation frequency, phase noise, and control voltage range. Additionally, optional constraints such as absolute maximum power consumption or the number of available phases (N_ϕ in (7)) can be included to narrow down the search space. While the proposed algorithm favors the candidate that consumes the smallest power consumption (P_{osc}), it also outputs a set of candidates that achieves the frequency, phase noise, and control voltage constraints with additional power overheads. This provides further opportunities to decide the final design among near-optimum candidates based on other metrics, such as

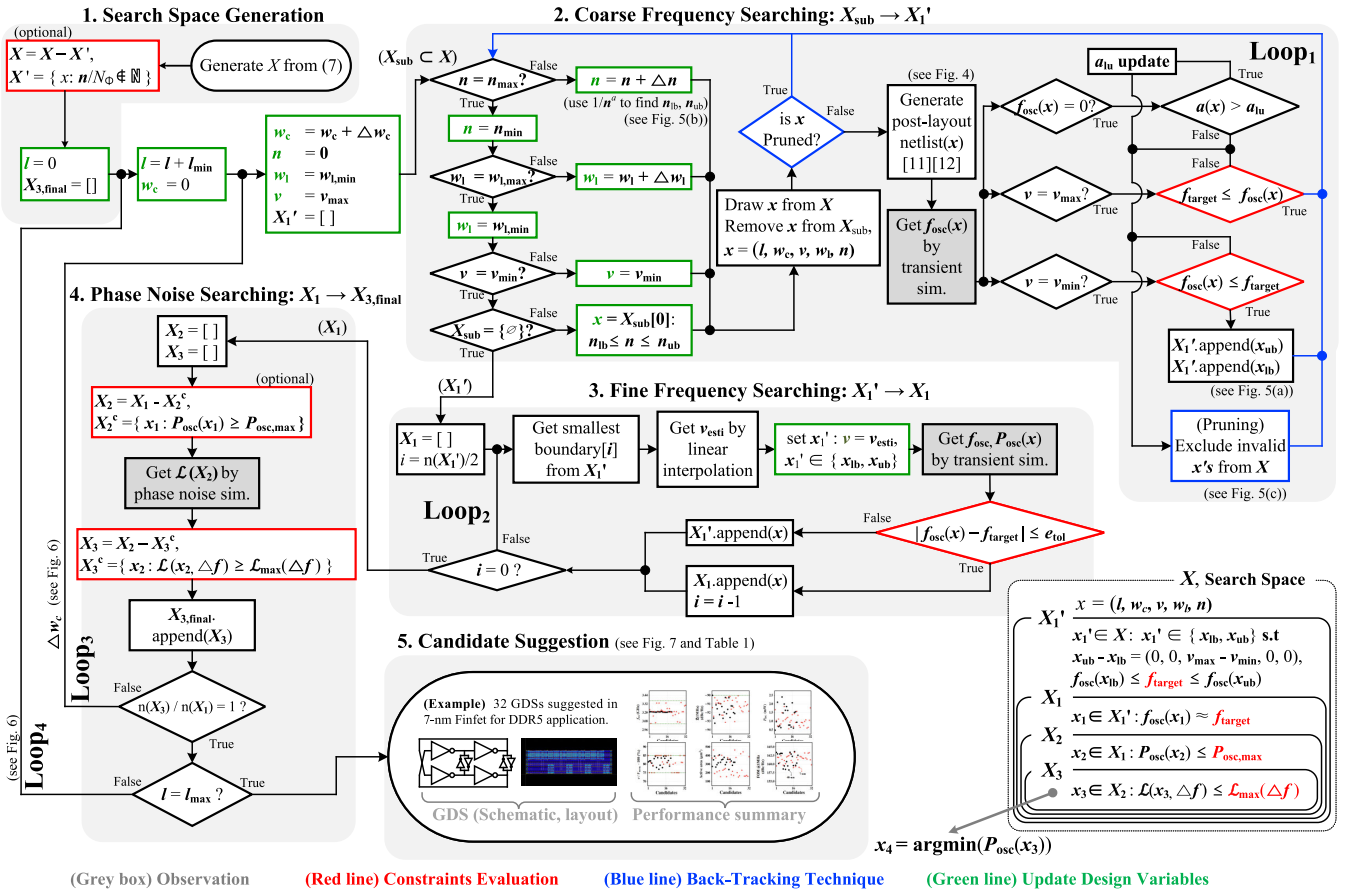


FIGURE 4. Flow chart of the proposed RVCO design automation.

oscillator FOM [19], area, and K_{VCO}.

$$\begin{aligned} &\text{Search: } x = (l, w_c, v, w_1, n) \in X \\ &\text{Minimize: } P_{osc}(x) \\ &\text{Subject to: } |f_{osc}(x) - f_{target}| < e_{tol} \\ &\qquad \mathcal{L}(x, \Delta f) \le \mathcal{L}_{max}(\Delta f) \\ &\qquad v_{min} \le v \le v_{max} \\ &\qquad (optional)\ P_{osc}(x) \le P_{osc,max} \\ &\qquad (optional)\ \phi(x)/N_\phi \in \mathbb{N} \end{aligned} \tag{7}$$

2) AUTOMATED DESIGN PROCESS

The overall RVCO design process is illustrated in Fig. 4. As mentioned in previous sections, the key idea of the proposed algorithm is to prevent running excessive simulations when exploring the search space composed of the five design variables. For this purpose, we construct five steps and four loops. First, we construct a five-dimensional search space X to be explored based on the design parameter vectors x (*Search Space Construction*). After that, candidates that satisfy the frequency constraint ($X_1 = \{x_1\}$) are discovered for each possible combination of l and w_c (*Coarse/Fine Frequency Searching*). The frequency search step is divided into the coarse/fine searching steps to efficiently exclude candidates that meet the frequency constraint without running simulations. In frequency searching, $loop_{1,2}$ sweep three design variables with measuring transient response for step purposes. The founded X_1 are then further examined by running phase noise simulations (*Phase-Noise Searching*). The searching direction is designed to minimize the number of time-consuming phase noise simulations. The frequency and phase noise searching steps are iterated over pairs of l and w_c though $loop_{3,4}$, while the scope and resolution of the iteration are dynamically adjusted for rapid searching. Finally, the candidates that meet the frequency and phase noise constraints ($X_{3,final} = \{x_3\}$) and the optimal candidate x_4 that achieves the lowest power consumption are suggested (*Candidate Suggestion*). Each step is elaborated on in the following paragraphs with examples.

Step 1. (Search Space Construction): During the first phase of the design process, we construct a 5-dimensional search space X composed of design parameter vectors $x = (l, w_c, w_1, n, v)$ to be explored. When the desired number of phases N_ϕ is provided, candidates that do not meet the phase requirements in (7) are dropped out. For example, for four-phased clock generation cases ($N_\phi = 4$), three, five, and seven stage oscillators are removed from the search space.

After the search set is constructed, the algorithm enters $loop_4$ and $loop_3$ to find out the candidates. Among the five

design parameters, only the channel length l is iterated over the full range ($loop_4$ in Fig. 4), as the oscillation frequency and phase noise characteristics vary significantly depending on the value of channel length. For each value of l, the core transistor width w_c is swept from its lowest value ($loop_3$ in Fig. 4), finding out candidates that meet the oscillation frequency and phase noise conditions.

Step 2. (Coarse Frequency Searching): As the first performance evaluation, the transient behavior is observed for searching X_1 that fulfills frequency requirements. The coarse frequency searching precedes before fine frequency searching for the selected values of l and w_c. The second step explores a 3-dimensional subspace $X_{sub} \subset X$. In other words, the 3-dimensional subspace is composed of vectors $x = (l_0, w_{c0}, w_1, n, v)$ when the pair (l_0, w_{c0}) are given, and only the maximum and minimum voltage is used in this step (v_{max} and v_{min} respectively).

Instead of fully exploring the subspace, monotonous properties of the oscillation frequency (with respect to n, w_1 and v) and the oscillation condition (with respect to w_1/w_c) are exploited to reduce the number of exploration. In particular, for the oscillation frequency of RVCOs, the following inequality is derived by (5),

$$f_{osc}(l_0, w_c, w_{l0}, n_0, v_0) \geq f_{osc}(l_1, w_c, w_{l1}, n_1, v_1) \quad \text{when } l_0 \leq l_1,\ w_{l0} \leq w_{l1},\ n_0 \leq n_1,\ v_0 \geq v_1 \tag{8}$$

where f_{osc} is the oscillation frequency on given x. As stated in the inequality, f_{osc} has negative partial derivatives for l, w_1, and n, and positive ones for v. This characteristic is also the reason for the separation of coarse and fine-frequency searching. As shown in Fig. 5(a) which shows the frequency with respect to the number of stages, the target frequency f_{target} must be surrounded by oscillation frequencies when v is v_{max} and v_{min}. It indicates that it forms the boundary where x_1 exists. We set a course search to find that boundaries X_1' (the collection of pair of upper and lower boundary x) and a fine search to sample X_1 from X_1' with sweeping v. As the exploration space where v is adjusted is reduced from X_{sub} to X_1', the computation can be reduced.

To sample X_1' from X_{sub}, three design variables are updated with the post-layout transient simulation in $loop_1$. It is ended when X_{sub} is explored completely. The algorithm first choose $v \in \{v_{max}, v_{min}\}$, then fix a valid value of w_1. Next, over the current parameters (l, w_c, w_1, v), it scan the valid values of n. Instead of iterating the whole possible values of n linearly, the proposed algorithm utilizes the $1/n$ dependency of f_{osc} (which is revealed in (5)). To be specific, as the oscillation period is roughly proportional to the number of stages, the value of n that yields the target oscillation frequency can be computed from the following expression:

$$n_{bnd} = \text{round}(\frac{f_{osc,start}}{f_{target}} \cdot n_{start})$$
$$n_{bnd} = n_{lb},\ n_{ub} \tag{9}$$

where $f_{osc,start}$ is the measured oscillation frequency at initial point ($n = n_{start}$, $v \in \{v_{max}, v_{min}\}$). n_{ub} and n_{lb} are correspond to the upper and lower boundary values of n based on the frequency constraint respectively. As the oscillation frequency slightly deviates from the estimated value from the $1/n$ dependency, several iterations are required to find out the actual values of n_{ub} and n_{lb}. To increase accuracy, we use the $1/n^{\alpha}$ model for the second estimation (see Fig. 5(b)). After the range of n is founded, the $\{x' : n_{lb} \leq n \leq n_{ub}\}$ are evaluated at the end of $loop_1$. This approach quickly finds X_1' where the target oscillation frequency is covered by the control voltage range (v_{max}, v_{min}). For example, the case illustrated in Fig. 5(b) takes 11 simulation steps to discover X_1' while the linear search would take 20 steps to get to the same point.

While searching the boundary values of n, based on the observations at the boundary conditions and the monotonicity in (8), x incapable of meeting the frequency constraint are excluded from the search list. This process is called pruning, as multiple candidates with related parameter values are removed from the search scope without any simulations. To be specific, if the measured oscillation frequency of a candidate is lower than f_{target} when $v = v_{max}$, candidates with a higher channel length l should not meet the oscillation frequency constraint when they share the same parameters except l with the measured candidate. Therefore, the candidates are pruned out without running actual simulations. The same property applies to w_1 and n (see Fig. 5(c)). It should be noted that the core inverter width w_c is not considered to have a monotonic dependency on the oscillation frequency, as its increase does not always lead to a higher oscillation frequency due to increased wiring capacitances. In addition to the frequency-based pruning, the allowable latch ratio for each value of (l, n) is estimated as well and exploited for the pruning process. When the post-layout simulation reveals that the current candidate is not strong enough for sustaining oscillation, its latch ratio is computed and all unexplored candidates with a smaller latch ratio than the current value are excluded from further explorations. The exclusion list is checked during each coarse frequency searching step to reduce the number of post-layout simulations.

Step 3. (Fine Frequency Searching): After figuring out the set of candidates (X_1' in Fig. 4), an additional process is performed to find the actual value of v that yields the oscillation frequency in $loop_2$. This step is called fine frequency searching. During the fine frequency searching process, the potential value of v is estimated from linear interpolation (of which initial interpolation seeds are provided from v_{max} and v_{min}). The oscillation frequency is then measured at the estimated control voltage, which is used for the next interpolation step. By iterating the interpolation process, the current design parameter vector x converges to the point that yields the target oscillation frequency f_{target} with its measured power consumption provided.

Step 4. (Phase-Noise Searching): After finishing the frequency searching step, we obtain the set of candidates that

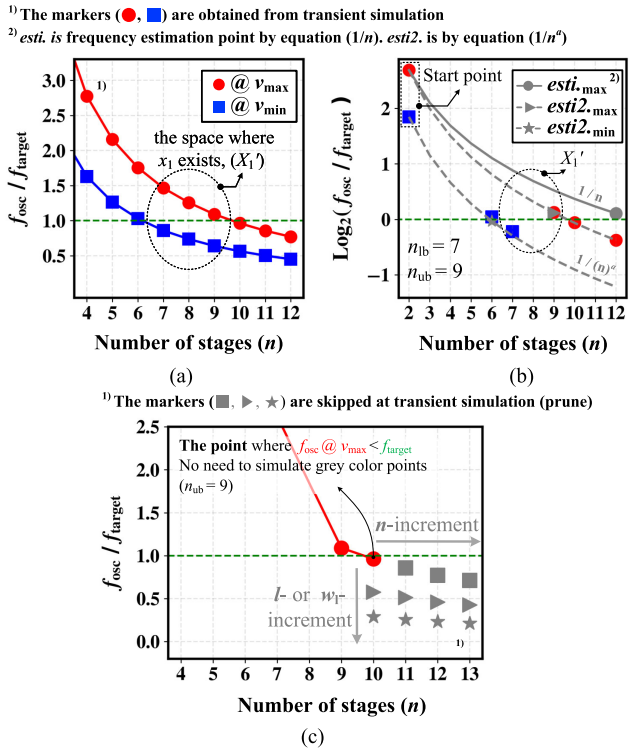


FIGURE 5. Examples of (a) the condition where x_1 satisfies the frequency constraints. (b) Finding n_{lb} and n_{ub} by using frequency estimations. (c) Pruning invalid x's that do not satisfy frequency constraints (grey markers) without running further simulations.

meet the frequency constraint (X_1 in Fig. 4). The vectors are then provided for the next step to find candidates that fulfill the phase noise performance, with an (optional) preclusion process based on the power consumption constraints. For the candidates that meet the frequency and power constraints, we run periodic-steady-state and phase noise simulations to measure their phase noise profile. If the phase noise performance does not meet the target specification, the candidate is discarded. After finishing the phase noise evaluations over candidates with current length and core inverter width parameters (l, w_c), the algorithm advances to the next value of w_c for further explorations. Instead of continuously sweeping the value of w_c, the step size is adaptively adjusted to boost the convergence speed, based on the number of candidates that pass the noise performance constraint among the candidates that meet the frequency constraint during the current trial. To be specific, the metric to determine the step size of w_c is defined as follows:

$$score = n(X_3)/n(X_2) \tag{10}$$

If the score is zero, a coarse step is applied to the increment of w_c because it indicates that there is no candidate that meets the phase noise constraint with the current value of w_c. This means the candidates dissipate too small power to achieve the phase noise constraint. As the value of w_c increases, some of their associated candidates meet the phase noise requirement, enhancing the score parameters ($0 < \text{score} < 1$), as illustrated in Fig. 6. Then the algorithm reduces the step size of w_c

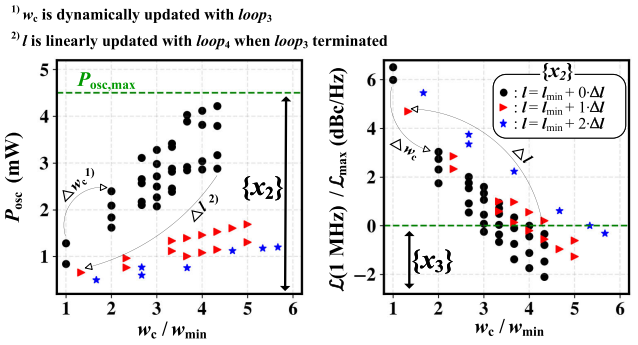


FIGURE 6. Process of finding x_3 in the phase noise searching step. All data points satisfy the frequency constraint. w_c is iterated in $loop_3$ and l is iterated in $loop_4$.

to find out near-optimal values of w_c and their associated candidates as possible. After the score becomes one (all candidates that meet the frequency constraint also meet the phase noise constraint), the $loop_3$ is terminated (optionally after a few additional trials) to avoid running unnecessary simulations to discover candidates with excessive phase noise performances. Fig. 6 shows the dynamic step adjustment for w_c sweep and its resulting candidate trajectories. As shown in the figure, more candidates meet the phase noise performance as the value of w_c increases (at the expense of additional power consumption). it receives a set of design parameter vectors (w_c, w_1, n, v) that achieve the target frequency and phase noise constraint for the current value of l. By repeating the candidate searching process over the entire range of l, the algorithm finally constructs a complete set of x for target constraints.

Step 5. (Candidate Suggestion): After the algorithm finishes the phase noise searching step, it outputs the optimal design vector x_4 that yields the lowest power consumption, together with other near-optimal candidates for further trade-off explorations. The example of candidate suggestions will be described in the next section.

IV. CASE STUDY: DDR5

In order to verify the proposed RVCO design methodology, RVCOs oscillating at the maximum clock rate (3.2 GHz) of DDR5 applications [24] in 40-nm and 7-nm technologies are produced. The target control voltage range is set to 75% and 85% of the nominal supply voltage, and the desired number of phases is set to 4 for the quadrature clock generation. The overall target specification is summarized as follows:

$$\begin{aligned}
&\text{search: } x = (l, w_c, v, w_1, n)\\
&\text{Minimize: } P_{osc}(x)\\
&\text{subject to: } f_{osc}(x) = 3.2\ \text{GHz with 5\% tolerance}\\
&\qquad\qquad \mathcal{L}(x,\ 1\ \text{MHz}) \ \leq\ -90\ \text{dBc/Hz}\\
&\qquad\qquad 75\% \cdot v_{\text{nominal}} \ \leq\ v \ \leq\ 85\% \cdot v_{\text{nominal}}\\
&\qquad\qquad (optional)\ \phi(x)/4 \ \in\ \mathbb{N}
\end{aligned} \tag{11}$$

The proposed method suggests 32 final candidates (including the best candidate that achieve the lower power consumption

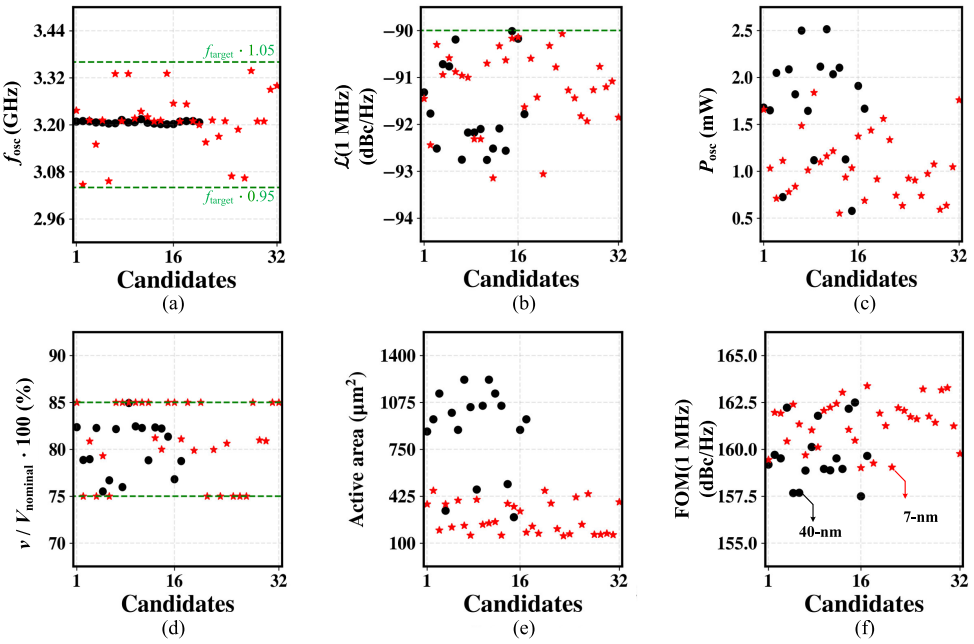


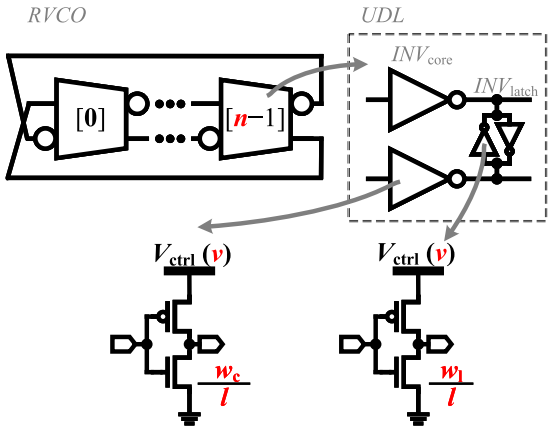
FIGURE 7. Application results of the proposed algorithm in 40-nm and 7-nm technology (Target specification; $\mathcal{L}_{max}$(1 MHz) = −90 dBc/Hz, f_{target} = 3.2 GHz with e_{tol} = 5%, Desired output phase number = 4). 17 and 32 candidates are found in the 40-nm planar CMOS and 7-nm FinFet, respectively. The resulting performance parameters are plotted: (a) f_{osc} (b) $\mathcal{L}$(1 MHz) (c) P_{osc} (d) Normalized control voltage (e) Active area (f) Oscillator FOM(1 MHz).

TABLE 1. Summary of output candidates from the proposed algorithm. Candidates 14 and 12 achieve the smallest power consumption (x_4) at 40-nm and 7-nm, respectively. Other candidates displayed in the table are optimal candidates with respect to various oscillator characteristics (bold text values).

Index of candidate	**14** (x_4)	14	10	14	14	**12** (x_4)	16	11	22	12
Technology (nm)	40	40	40	40	40	7	7	7	7	7
Core/Latch length, l (nm)[1]	120	120	40	120	120	24	24	24	32	24
Core width, w_c (μm)[2]	8.64	8.64	10.0	8.64	8.64	4.6	6.1	6.7	9.2	4.6
Control voltage, v (mV)	772.9	772.9	781.7	772.9	772.9	609.2	608.2	637.5	562.5	609.2
Latch width, w_l (μm)[2]	4.32	4.32	4.32	4.32	4.32	0.5	0.5	1.5	4.6	0.5
Number of stages	2	2	8	2	2	4	4	4	2	4
Frequency (GHz)	3.20	3.20	3.208	3.20	3.20	3.21	3.21	3.22	3.17	3.21
P_{osc} (mW)	**0.57**	0.57	2.51	0.57	0.57	**0.55**	0.69	1.22	0.633	0.55
FOM (dBc/Hz)[3, 4]	162.5	**162.5**	158.8	162.5	162.5	163.0	**163.4**	162.4	162.1	163.0
$\mathcal{L}$ (1 MHz) (dBc/Hz)[3]	–90.0	–90.0	**–92.75**	–90.0	–90.0	–90.3	–91.6	**–93.1**	–90.1	–90.3
Active area (μm^2)	279	279	1233	**279**	279	153	175	248	**150**	153
K_{VCO} (GHz/V)[5]	9.5	9.5	7.4	9.5	**9.5**	6.4	6.2	5.2	6.4	**6.4**

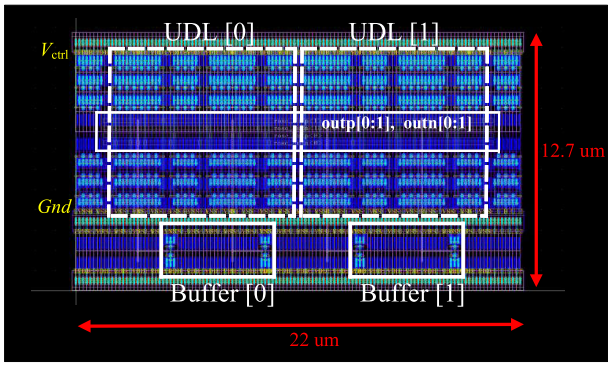
[1] Designed in stacked device rather than single device.
[2] Sum of the widths of NMOS and PMOS.
[3] Measured at the frequency offset of 1 MHz.
[4] FOM = $-\mathcal{L}(\Delta f) + 20\log_{10}(f_{osc}/\Delta f) - 10\log_{10}(P_{osc}/1\text{mW})$ [23].
[5] The largest K_{VCO} is chosen for entire frequency range.

for each technology) in 7-nm technology and 17 candidates in 40-nm technology. In 7-nm technology, it takes 690 transient simulations, 355 parasitic extractions, and 55 phase noise simulations. In 40-nm technology, it takes 201 transient simulations, 119 parasitic extractions, and 23 phase noise simulations. Fig. 7 shows the characteristics of the output candidates in 40nm (black dots) and 7nm (red stars) technologies. All selected candidates meet the target specification with 5% tolerance in frequency error. The power consumption does not include additional circuits for the control voltage generation (such as voltage regulator), as the circuit topologies vary significantly across designs. It is worth mentioning that the Oscillator Figure of Merit (FOM) does not improve with technology scaling. Among them, the candidate that achieves the smallest power consumption is suggested, while all other candidates are summarized for the designer's consideration as shown in Table 1. Fig. 8 shows a schematic with the lowest power consumption candidate parameters in each technology and the layout in 40-nm technology. By utilizing the proposed methodology, we can analyze the relationship between design



Tech. (nm)	Index	l (nm)	w_c (μm)	v (mV)	w_l (μm)	n
40	14	120	8.64	772.9	4.32	2
7	12	24	4.6	609.2	0.5	4

(a)



(b)

FIGURE 8. (a) The schematic with design variables of the smallest power consumption candidate in 40-nm and 7-nm technology. The buffer circuit is omitted (see Fig.4 for detail) (b) The generated layout of the smallest power consumption candidate in 40-nm technology (index = 14).

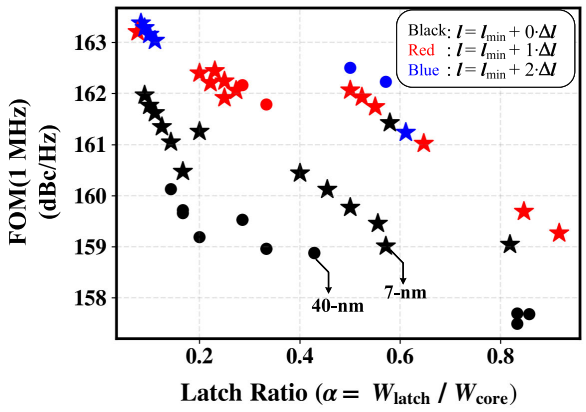


FIGURE 9. FOM versus latch ratio (α) of output candidates selected from the proposed algorithm. Circle and star markers stand for 40-nm and 7-nm candidates, respectively. Colors stand for normalized device length.

variables and the performance of candidates. Fig. 9. shows the relationships between the FOM and design variables: latch ratio (w_l/w_c) and l. The definition of FOM is defined in Table 1. From Fig. 9, it is observed that to design low-phase noise with low power consumption at the identical frequency, the device length should get larger and the latch ratio should get smaller, which is consistent with [19].

V. CONCLUSION

In this paper, we present an automated design methodology for a ring voltage-controlled oscillator. The proposed methodology explores the design spaces and finds the candidates that meet the target specification items, by automatically generating sized schematics and layouts, and running post-layout simulations iteratively. The number of post-layout simulations is reduced by utilizing the nature of ring oscillators and intermediate explorations results to exclude unsuitable candidates without running simulations. The method is applied to generate RVCOs in 40-nm and 7-nm CMOS technologies for DDR5 applications. The optimal candidates achieve 0.57 mW power consumption in 40-nm technology and 0.55 mW power consumption in 7-nm technology at 3.2 GHz.

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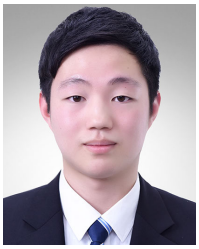

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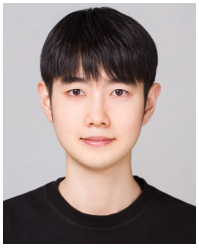

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