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Ultra-High-Image-Density, Large-Size Organic Light-Emitting Device Panels Based on Highly Reliable Gate Driver Circuits Integrated by Using InGaZnO Thin-Film Transistors

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ABSTRACT Large-size, organic light-emitting device (OLED) panels based on highly reliable gate driver circuits integrated using InGaZnO thin-film transistors (TFTs) were fabricated to achieve ultra-high image density (UHD). These large-size OLED panels were driven by using a novel gate driver circuit not only for displaying images but also for sensing TFT characteristics for external compensation. Regardless of the negative threshold voltage of the TFTs, the proposed gate driver circuit in OLED panels functioned precisely, resulting from a decrease in the leakage current. The falling time of the circuit is approximately 1.6 μs, which is fast enough to drive UHD OLED displays at 120 Hz. 120 Hz is most commonly used as the operating voltage because images consisting of 12 frames per second can be quickly shown on the display panel without any image sticking. The reliability tests showed that the lifetime of the proposed integrated gate driver is at least 1×10^5 h.

INDEX TERMS Organic light-emitting devices, ultra-high-image density, large-size, gate driver, InGaZnO thin film transistor.

I. INTRODUCTION

Recently, with rapid advances in organic light-emitting device (OLED) technologies, the fabrication of large-size televisions (TVs) based on OLED panels [1], [2], which have been replaced by liquid crystal displays (LCDs) in the high-end market, has become possible. OLED panels with self-luminous sub-pixels simultaneously achieve perfect black without light leakage, and have high brightness, a much wider viewing angle, and higher luminance uniformity due to advanced compensation technologies [3], [4]. However, OLED panels because of their high price are not sufficiently competitive to replace LCDs. In order to reduce cost of OLED panels, the cost-reduction technologies in addition to the current quality-oriented technologies are required to gain a higher market share [5]. LCDs have a long history of using cost-reduction technologies, including the use of integrated gate driver circuits that eliminate gate driver ICs and can have a narrow bezel size [6]–[9]. Gate driver integration is one of the key technologies for flexible displays and tiling displays, and the utilization of gate driver circuits has become necessary for OLED panels [10], [11].

Oxide thin-film transistors (TFTs), which are different from the a-Si TFTs commonly used for LCDs, are currently being used as backplanes for OLED display [12]. Because the mobilities of oxide TFTs are approximately 10 times higher than those of a-Si TFTs, the integrated circuits tend to be smaller. On the other hand, depletion-mode transistors often have a negative threshold voltage (Vth) at an initial stage, which will result in a leakage current and even a malfunction if the transistors are not well designed [13], [14]. While the resistance of an oxide TFT to a positive bias is typically larger than that of a-Si TFT, the recovery of

the Vth of the oxide TFT is generally slow, and its shift in real situations does not show a saturation behavior [15]. Therefore, these disadvantages should be taken into account when designing integrated circuits with oxide TFTs.

This paper presents new technological approaches to resolving those issues, related to the fabrication of oxide-based integrated gate driver circuits for use in OLED panels and introduces the latest products fabricated utilizing such integrated circuits. The characteristic issues of the oxide TFT are improved by using the design approaches of the circuit with the gate driver.

II. INTEGRATED GATE DRIVER CIRCUIT DESIGN

Active-matrix displays basically require gate ICs for the horizontal gate lines and source ICs for the vertical source lines. Because the gate signals generally have only two kinds of states, high and low states, the integration of the gate circuit is simpler than that of the source circuit for satisfying performance requirements. Because the active-matrix display should be replaced by high-mobility Si-based ICs [16], [17], double-rate driving and triple-rate driving methods for LCDs have already been developed and applied to products in order to reduce the cost of the source ICs [18], [19].

Since the OLED panels require sophisticated sensing and compensation, unlike LCDs with a simple gate driving circuit [20], the integration of the gate driver in the OLED panels is very difficult. In addition to the sequential drive of the gate lines, the sensing function of the V_{th} and the mobility are necessary for the TFTs if the OLED panels are to operate properly [21]. Because the pixels with low V_{th} values are rapidly degraded due to the large current flow which results in the decrease of the lifetime of the OLED panels, the flow current of the pixels should be constant [22]. This occurs due to the rapid change in temperature when the flow current is not a constant. Degradation may increase when high temperature condition because higher current flows as the mobility in the TFT increases which accordingly increases the current density in the TFT with low Vth.

Any gate driver circuit proposed for use in OLED panels should have dedicated blocks for sensing, and a method for driving the scan and the sense lines with different times is essential for the design of a novel gate driver circuit for use in highly efficient OLED panels [23].

Figure 1 shows a schematic diagram of the proposed integrated gate driver circuit for use in OLED panels. The dual pull-down structure is controlled by each of the two Qb-nodes. Only one of the two pull-down TFTs is used to suppress the V_{th} shift by reducing the duty ratio to 50%. Because oxide TFTs are depletion-mode TFTs with negative V_{th} values, leakage currents might cause malfunction, especially in the sensing mode, which the pulse width is much larger than that of the display mode [24]. The channel length, mobility, V_{th} center value, and maximum distribution of the manufactured a-IGZO TFT is 5.5 μm, 9.5 cm^2/v.s, 0.05 V, and 0.57 V, respectively. The manufactured TFT showed excellent uniformity, but negative V_{th} when considering the

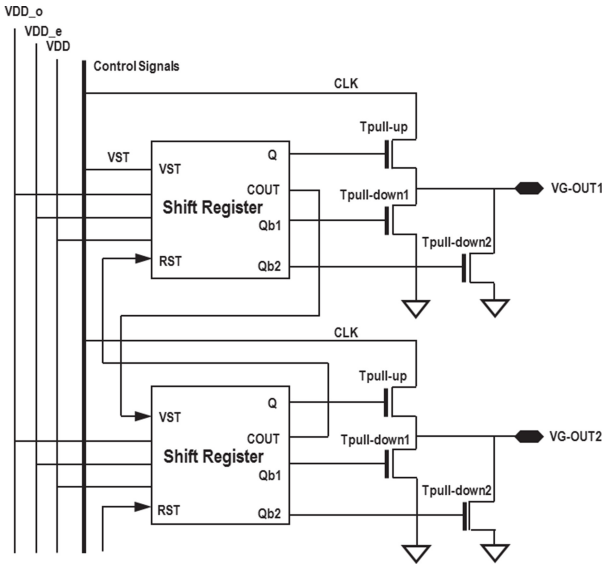

FIGURE 1. Schematic diagram of the proposed integrated gate driver for OLED panels.

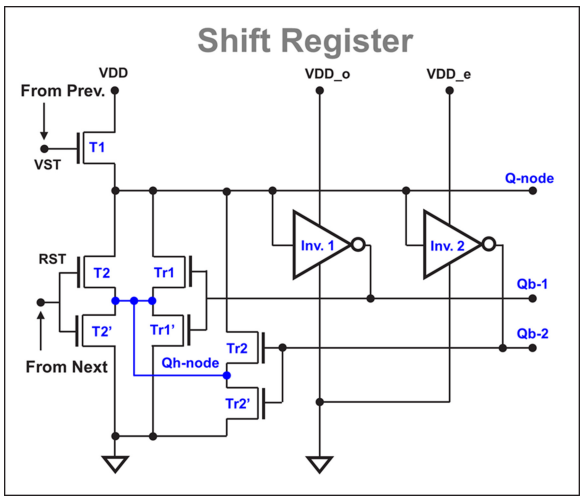

FIGURE 2. Schematic diagram of the shift register block with a dual pull-down structure.

distribution characteristics. By applying bias voltage to the source higher than the gate when the TFT is off, circuit errors can be prevented by eliminating the leakage current of the TFT if V_{gs} ($V_g - V_s$) is maintained lower than the negative V_{th} of the TFT. The average power consumption of the gate driver at 24 V/−6 V operation was 900 mW.

The leakage current can be successfully suppressed by adding the Qh-node, as shown in Fig. 2. The Q-node is not directly connected to the low-voltage line via any TFT; the node is connected only to the Qh-node, which is automatically connected to the low-voltage line. The Qb-node and the Qh-node always have the same voltage, and the operation of the TFTs between two different nodes at high voltages can be turned off safely even when the V_{th} value of the TFT is negative.

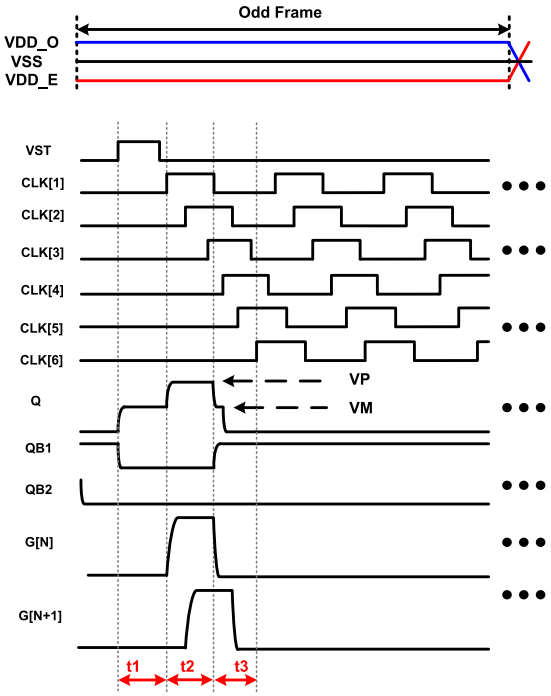

FIGURE 3. Timing diagram of the proposed integrated gate driver circuit in the display mode.

Figure 3 shows the timing diagram of the proposed integrated gate driver circuit in the display mode. The timing diagram in the display mode can be described as follows: the voltage of the scan start signal (V_{ST}) increases during the period t_1, charges the buffer of the TFT (T_{pu}) gate line through the SR latch, and increases the Q-node voltage. Then, T_{pu} is turned on, which resets the gate line to CLK1, and the V_{ST} signal transfers from high to low voltage, thereby blocking the charging of the Q-node. The Q-node voltage can be maintained at the clock's high voltage level because of the existence of the capacitance of the buffer TFT. The V_{ST} signal during the period t_2 transfers CLK from low to high voltages. Then, the Q-node voltage is bootstrapped, and the T_{pu} starts to charge the gate line to the high level of the CLK voltage and turns on the TFTs in the active region to charge the pixel capacitor. After the pixel charging has been completed, the selected gate line is discharged to turn off the TFTs in the active region before the (N+3) gate line is charged by the CLK4 transition to the high level of the CLK voltage during the period t_3 because the gate line, by means of the CLK transition to the low voltage level at the CLK non-overlap time between the CLK1 and the CLK4, is discharged. When the CLK transition to low voltage occurs in advance of the CLK4 transition to high voltage, the gate line is discharged by the CLK1 through the T_{pu} during the period t_3 until the CLK4 transition turns on the next gate output and then turns on the Tpd to turn off the Tu. When the clock's duty ratio starts to decrease from 50%, part of the discharging gate line can be transferred to the T_{pu}. The lower the duty ratio is, the more the gate line is discharged by using the T_{pu}, resulting in decreased T_{pd} size.

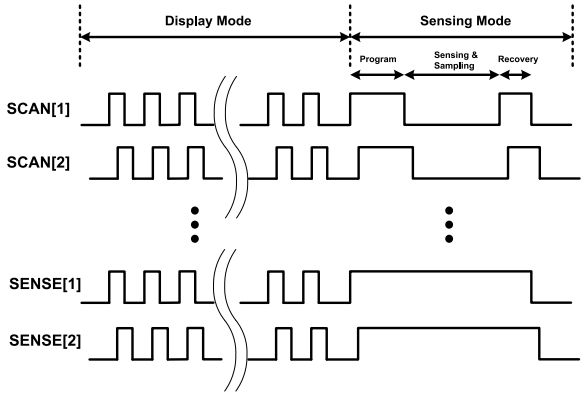

FIGURE 4. Timing diagram of the proposed integrated gate driver circuit in the sensing mode.

Figure 4 shows the timing diagram of the proposed integrated gate driver in the sensing mode. The signal width for the gate driver in the sensing mode is larger than that when it is in the display mode. The pulse signal of the gate driver does not deteriorate over a long time, which plays an important role in obtaining reliable OLED panels.

III. RESULTS AND DISCUSSION

The lifetimes of the integrated driver circuits are very important if they are to replace the ICs currently used in the relatively unstable TFTs in OLED panels [25]. While the lifetime of an OLED gradually deteriorates, that of an integrated circuit suddenly malfunctions like a light bulb. Thus, it is important not only to design a highly reliable integrated circuit but also to estimate its lifetime correctly. The deterioration of the pull-down TFTs with the fastest V_{th} shift rates should be correctly measured by using a nondestructive method [26]. When the V_{th} of the pull-down TFTs becomes higher than the V_{DD} voltage, the TFTs can no longer hold a gate line at low voltage, resulting in a circuit malfunction. The clamping voltage and the lowest operating voltage of the V_{DD} line have been used to estimate the V_{th} of the pull-down TFTs. Because lowering the V_{DD} voltage has an effect similar to that of a positive V_{th} shift of the pull-down TFTs, a voltage margin can be estimated before the malfunction of the circuit. After the reliability tests, the V_{th} of each TFT can be measured by using a destructive method to confirm that the V_{th} of the pull-down TFTs is the dominant factor. Because the V_{th} of the pull-down TFTs can be estimated by the lowest operating voltage of the V_{DD} line, the Vth of the pull-down TFTs is preferable than that of the pull-up TFTs.

A scalable integrated gate driver circuit with a sensing function has been successfully developed, and the driver circuit has been applied to 55-inch UHD OLED displays. The product lifetimes of the highly reliable OLED displays with a dual pull-down structure have been measured. Figure 5 shows the internal voltages as functions of time for the Q-node and the gate output states. The fall time of the circuit

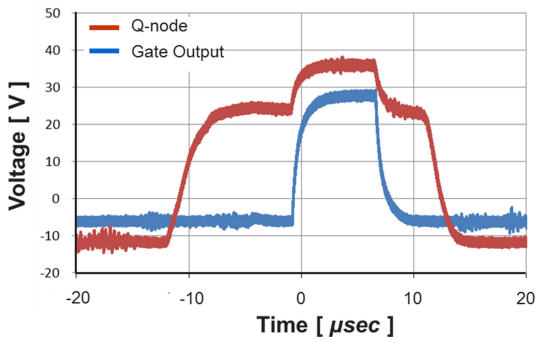

FIGURE 5. Experimental voltages as functions of time for the integrated gate driver.

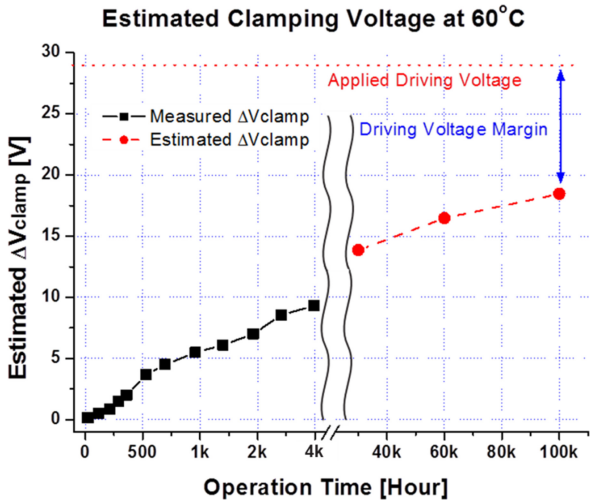

FIGURE 6. Measured and estimated clamping voltages under an acceleration life test at 60°C.

is approximately 1.6 μs, which is fast enough to drive UHD OLED displays at 120 Hz. Because the gate on-time of the UHD OLED displays is 3.6 μs, their fall times should be 1/2 to charge and discharge within the time.

Figure 6 shows the measured and the estimated clamping voltages under an accelerated life test at 60°C. The results of the reliability test show that the lifetime of the proposed integrated gate driver is at least 1×10^5 h. The Vth shift for the OLED display does not saturate until an operation time of 1×10^5 h. Because the product guarantee time of the OLED displays is 3×10^4 h, the deterioration of our device is slow enough for practical applications in OLED displays. A microscopic image of the integrated gate driver on the bezel, indicative of a well-organized circuit layout, is depicted in Fig. 7. While the input clock signal is located on the left, the circuit for the control logic and the buffer TFT are located on the right.

Figure 8 shows a photograph of the 55-inch UHD OLED panel with an integrated gate driver circuit. OLED panels are designed as bottom-emission-type panels by using oxide TFT backplanes, and they achieve the characteristics of a narrow bezel (5.5 mm) by utilizing an integrated gate driver. The

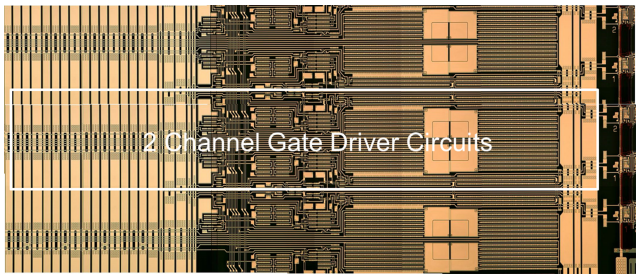

FIGURE 7. Microscopic image of the bezel of the integrated gate driver on the 55-inch UHD OLED panel with the proposed integrated gate driver.

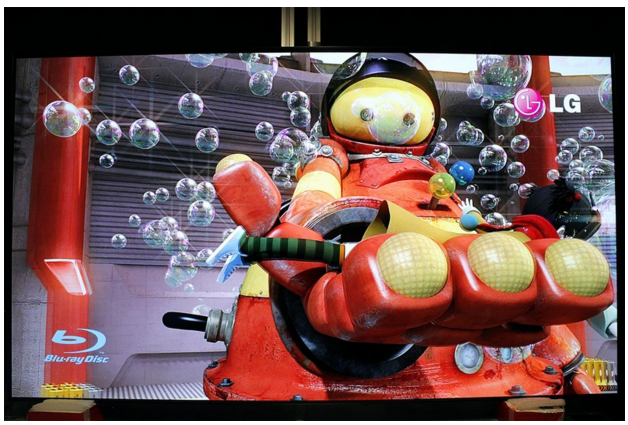

FIGURE 8. The 55-inch UHD OLED panel with the proposed gate driver integrated using IGZO TFTs.

TABLE 1. Device performance of the 55-inch OLED displays with a gate driver integrated panel.

Item	Content	Unit
Panel size	55, 65	inch
Resolution	3840×2160 (UHD)	—
Frame rate	120	Hz
Bezel Size	5.5	mm
Brightness	> 500	cd/m^2
Contrast ratio	> 1,000,000 : 1	—
Panel Structure	2G-1D	—

performance parameters of the 55-inch OLED panels are detailed in Table 1. These parameters, functionalities of the sensing and the compensation of the OLED panels, can be seen to be the same as those of OLED panels with the previously used gate ICs.

IV. CONCLUSION

An integrated gate driver circuit for use in large-size OLED displays with sensing functions and scalability was developed to achieve UHD OLED displays. The lifetime of the proposed integrated gate driver is at least 1×10^5 h. The designed gate drive circuit precisely operated in the OLED panels, regardless of the negative threshold voltage of the TFTs. The falling time of the circuit is approximately 1.6 μs, which is fast enough to drive UHD OLED displays at 120 Hz. These results indicate that the gate driver circuit integrated

by using InGaZnO TFTs holds promise for application in large-size UHD OLED.

REFERENCES

[1] H. J. Shin and T. W. Kim, "Ultra-high-image-density large-size organic light-emitting devices based on In–Ga–Zn–O thin-film transistors with a coplanar structure," *Opt. Exp.*, vol. 26, no. 13, pp. 16812–16819, Jul. 2018.

[2] X. Luan, J. Liu, Q. Pei, G. C. Bazan, and H. Li, "Gate-tunable electron injection based organic light-emitting diodes for low-cost and low-voltage active matrix displays," *ACS Appl. Mater. Interfaces*, vol. 9, no. 20, pp. 16750–16755, May 2017.

[3] Y. H. Jang, "Instability of shift register circuits using hydrogenated amorphous Si TFTs," *Jpn. J. Appl. Phys.*, vol. 45, pp. 6806–6811, Sep. 2006.

[4] W. B. Jackson, J. M. Marshall, and M. D. Moyer, "Role of hydrogen in the formation of metastable defects in hydrogenated amorphous silicon," *Phys. Rev. B, Condens. Matter*, vol. 39, p. 1164, Jan. 1989.

[5] H. Lebrun, N. Szydlo, and E. Bidal, "Threshold-voltage drift of amorphous silicon TFTs in integrated drivers for active matrix LCDs," *J. Soc. Inf. Display*, vol. 11, no. 3, pp. 539–542, Sep. 2003.

[6] C.-L. Lin, P.-S. Chen, M.-Y. Deng, C.-E. Wu, W.-C. Chiu, and Y.-S. Lin, "UHD AMOLED driving scheme of compensation pixel and gate driver circuits achieving high-speed operation," *IEEE J. Electron Dev. Soc.*, vol. 6, no. 1, pp. 26–33, Oct. 2018.

[7] M. Mativenga, M. H. Choi, J. W. Choi, and J. Jang, "Transparent flexible circuits based on amorphous-indium–gallium–zinc–oxide thin-film transistors," *IEEE Electron Device Lett.*, vol. 32, no. 2, pp. 170–172, Feb. 2011.

[8] G. W. Chang *et al.*, "Temperature-dependent instability of bias stress in InGaZnO thin-film transistors," *IEEE Trans. Electron Devices*, vol. 61, no. 6, pp. 2119–2124, Jun. 2014.

[9] W.-J. Wu *et al.*, "A highly stable biside gate driver integrated by IZO TFTs," *IEEE Trans. Electron Devices*, vol. 61, no. 9, pp. 3335–3338, Sep. 2014.

[10] L.-R. Zhang *et al.*, "A low-power high-stability flexible scan driver integrated by IZO TFTs," *IEEE Trans. Electron Devices*, vol. 63, no. 4, pp. 1779–1782, Apr. 2016.

[11] J. W. Choi, J. I. Kim, S. H. Kim, and J. Jang, "Highly reliable amorphous silicon gate driver using stable center-offset thin-film transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2330–2334, Sep. 2010.

[12] C.-L. Lin, C.-D. Tu, M.-C. Chuang, and J.-S. Yu, "Design of bidirectional and highly stable integrated hydrogenated amorphous silicon gate driver circuits," *J. Display Technol.*, vol. 7, no. 1, pp. 10–18, Jan. 2011.

[13] C.-L. Lin, M.-H. Cheng, C.-D. Tu, C.-C. Hung, and J.-Y. Li, "2-D–3-D switchable gate driver circuit for TFT LCD applications," *IEEE Trans. Electron Devices*, vol. 61, no. 6, pp. 2098–2105, Jun. 2014.

[14] C.-L. Lin, M.-H. Cheng, C.-D. Tu, C.-E. Wu, and F.-H. Chen, "Low-power a-Si:H gate driver circuit with threshold-voltage-shift recovery and synchronously controlled pull-down scheme," *IEEE Trans. Electron Devices*, vol. 62, no. 1, pp. 136–142, Jan. 2015.

[15] B. Kim *et al.*, "A novel depletion-mode a-IGZO TFT shift register with a node-shared structure," *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 1003–1005, Jul. 2012.

[16] J. E. Pi *et al.*, "A low-power scan driver circuit for oxide TFTs," *IEEE Electron Device Lett.*, vol. 33, no. 8, pp. 1114–1146, Aug. 2012.

[17] C.-H. Chiang and Y. Li, "A novel driving method for high-performance amorphous silicon gate driver circuits in flat panel display industry," *J. Display Technol.*, vol. 12, no. 10, pp. 1051–1056, Oct. 2016.

[18] C.-L. Lin, F.-H. Chen, W.-C. Ciou, Y.-W. Du, C.-E. Wu, and C.-E. Lee, "Simplified gate driver circuit for high-resolution and narrow-bezel thin film transistor liquid crystal display applications," *IEEE Electron Device Lett.*, vol. 36, no. 8, pp. 808–810, Aug. 2015.

[19] C.-L. Lin, F.-H. Chen, M.-X. Wang, P.-C. Lai, and C.-H. Tseng, "Gate driver based on a-Si:H thin-film transistors with two-step-bootstrapping structure for high-resolution and high-frame-rate displays," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3494–3497, Aug. 2017.

[20] C.-L. Lin, C.-E. Wu, F.-H. Chen, P.-C. Lai, and M.-H. Cheng, "Highly reliable bidirectional a-InGaZnO thin-film transistor gate driver circuit for high-resolution displays," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2405–2411, Jun. 2016.

[21] Z. Hu, C. Liao, W. Li, L. Zeng, C. Y. Lee, and S. Zhang, "Integrated a-Si:H gate driver with low-level holding TFTs biased under bipolar pulses," *IEEE Trans. Electron Devices*, vol. 62, no. 12, pp. 4044–4055, Dec. 2015.

[22] H. J. Shin and T. W. Kim, "Enhancement of the luminance uniformity in large-size organic light-emitting devices based on In–Ga–Zn–O thin-film transistors by using a new compensation method," *IEEE J. Electron Devices Soc.*, vol. 7, no. 1, pp. 557–560, May 2019.

[23] B. Kim *et al.*, "New depletion-mode IGZO TFT shift register," *IEEE Electron Device Lett.*, vol. 32, no. 2, pp. 158–160, Feb. 2011.

[24] B. Kim *et al.*, "A depletion-mode a-IGZO TFT shift register with a single low-voltage-level power signal," *IEEE Electron Device Lett.*, vol. 32, no. 8, pp. 1092–1094, Aug. 2011.

[25] J. M. Lee, I. T. Cho, J. H. Lee, and H. I. Kwon, "Bias-stress-induced stretched-exponential time dependence of threshold voltage shift in InGaZnO thin film transistors," *Appl. Phys. Lett.*, vol. 93, no. 9, pp. 1–3, Sep. 2008.

[26] K.-S. Son *et al.*, "The effect of dynamic bias stress on the photon-enhanced threshold voltage instability of amorphous HfInZnO thin-film transistors," *IEEE Electron Device Lett.*, vol. 32, no. 2, pp. 164–166, Feb. 2011.