



Ultra-high-image-density large-size organic light-emitting devices based on In-Ga-Zn-O thin-film transistors with a coplanar structure

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Abstract: Drain currents as functions of the gate voltages for the thin-film transistors (TFTs) showed that their output currents had slight differential variations in the saturation region just as the output currents of the etch stopper TFTs did. The maximum difference in the threshold voltages for the In-Ga-Zn-O (a-IGZO) TFTs was as small as approximately 0.57 V. The color gamut of organic light-emitting devices (OLEDs) embedded with TFTs with a coplanar structure satisfied the digital cinema initiatives of 99%. Furthermore, the image density of large-size OLEDs embedded with TFTs with a coplanar structure was significantly enhanced in comparison with that of OLEDs embedded with conventional TFTs.

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1. Introduction

Recently, organic light-emitting devices (OLEDs) have been extensively used in promising applications, such as mobile phones, laptop computers, monitors, televisions, car displays, light sources, and public displays [1, 2]. OLEDs have emerged as excellent candidates for next-generation displays, having progressively replaced liquid crystal displays (LCDs) in high-resolution display systems, because OLEDs have self-luminous pixels that overcome the disadvantage of LCDs, which have thick, heavy, back light units (BLUs). OLEDs are thinner and have lighter weight, a wider viewing angle, and a much higher contrast ratio in comparison with LCDs [3, 4].

Much research has been focused on optimizing thin-film transistors (TFTs) based on semiconductor materials as a way to enhance the performances of large-size OLEDs [5,6]. Among the various amorphous-oxide materials, amorphous In-Ga-Zn-O (a-IGZO) thin films have been predominantly considered due to their having significant advantages, such as compatibility with the amorphous silicon process in large-area mass production, high mobility, and both short- and long-range uniformity [7, 8]. Demands for high-performance, high-resolution, and large-size OLEDs have been dramatically increasing with increasing requirements for high-quality image density. Although several inherent problems limit the ability to achieve ultrahigh image density from a large-size OLED, if such an image density were to be achieved using a large-size OLED, that would play an important role in making large-size display systems more practical [9].

Amorphous silicon TFTs (a-Si TFTs) with a high uniformity have been extensively utilized in the fabrication of large-size LCDs. However, the low mobility and the large

threshold voltage (V_{th}) shift of a-Si TFTs make their use as reliable backplanes for OLEDs difficult [10]. Low-temperature poly-silicon (LTPS) TFTs, which have superior characteristics including high mobility and high stability, are currently being used for small-size OLEDs [11]. However, the use of LTPS TFTs with poor uniformity in large-size OLEDs is difficult unless an additional complicated compensation pixel is included, but the inclusion of such a pixel would decrease the yield rate of mass production [12]. To the contrary, IGZO TFTs can be conveniently manufactured using the existing amorphous Si TFT process line. Even though some investigations on the device performances of conventional TFTs used in displays have been conducted [13–16], studies on the achievement of ultra-high-image-density (UHID) large-size OLEDs containing a-IGZO TFTs with a coplanar structure have not yet been performed.

This paper presents data demonstrating the achievement of an UHID from large-size OLEDs based on a-IGZO TFTs with a coplanar structure. The a-IGZO TFTs with a coplanar structure were fabricated so as to enhance their uniformity and reliability. Drain currents were measured as functions of the gate voltages for the a-IGZO TFTs to investigate the uniformity of their threshold voltages. Drain currents were also measured as functions of the drain voltages to investigate the saturation characteristics of the currents for the TFTs. Moreover, the drain currents for TFTs that had been subjected to a voltage bias or a current stress were measured as functions of the gate voltages to investigate their current fluctuations and stabilities. Finally, the performance of large-size OLEDs embedded with TFTs with a coplanar structure in producing UHID was investigated.

2. Experimental details

The detailed structure of the etch-stopper-layer (ESL)-type TFTs with a double gate formed by placing gates on the top and the bottom regions of the active layer is described elsewhere [17]. The ESL is necessary to protect the active film against the introduction of contaminants, which might deteriorate the reliability of oxide TFTs, so that a TFT with high performance can be achieved [18–22]. The TFTs with the ESL structure generate large parasitic capacitances between the gates and the drain/source metals.

TFTs with a coplanar structure were fabricated to overcome the drawbacks of the ESL-type TFTs and to satisfy image-density requirements for potential applications in large-size OLEDs. A cross-sectional view of such a self-aligned thin-film transistor with a coplanar structure containing a top gate is shown in Fig. 1. Novel technologies that were adopted for use in this fabrication process included the fabrication of top gate TFTs without overlap between metals, selective metallization of the active layer in the source/drain regions, and the formation of a light shield layer. First, the active layer of the a-IGZO film was formed by using a direct-current sputtering method, after which it was patterned by using a wet-etching method. The gate dielectric materials were formed by using plasma-enhanced chemical-vapor deposition, followed by the growth of a bilayer of MoTi and Cu as a gate electrode. After the gate electrode had been etched in a wet-bath, the gate insulator was dry-etched by using a photoresist of the gate pattern. The concentration of oxygen vacancies in the plasma-treated area was much larger than that in the non-treated area. Oxygen vacancies were easily generated near the surface of the a-IGZO region due to the plasma treatment and were later filled with oxygen from the environment during annealing or the formation of the SiO₂ layer. The plasma-treated a-IGZO surface on the source/drain region was formed by using dry etching. The sheet resistance of the a-IGZO on the source/drain region was decreased. The parasitic capacitance of the TFT was dramatically reduced by adopting a top gate TFT and a self-aligned conductive active layer in the source and drain regions. TFTs with a highly conductive a-IGZO film are necessary if the contact resistance is to be reduced and the current flow enhanced [23, 24]. Because the superfluous capacitance of the TFTs interrupts the effective operation of large-size OLEDs and has an adverse impact on their performance, a coplanar structure and an optimized heat process were adapted to improve the reliability of the TFTs [25, 26].

The reliability of the values of the V_{th} for the TFTs was characterized by using both an in-line probe station and an automatic sensing method. Test element groups (TEGs) with transistors at many sites on the glass substrates were monitored by using an in-line probe station. Additionally, the values of the V_{th} were determined for the TFTs for all pixels inside the UHID panel by using a real-time automatic V_{th} sensing method.

3. Results and discussion

Figure 1 shows the cross-sectional view of a self-aligned thin-film transistor with a coplanar structure containing a top gate.

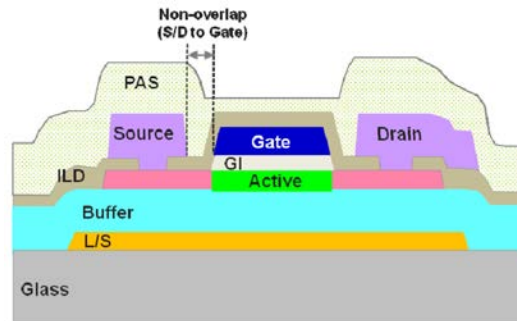


Fig. 1. Cross-sectional view of a self-aligned thin-film transistor with a coplanar structure containing a top gate.

The active layers in the coplanar TFTs, except for the gate mask, were exposed to plasma treatments, resulting in the formation of a highly conductive region. The results from Rutherford backscattering spectrometry performed on the plasma-treated active layer demonstrated that the amount of oxygen at the surface of the active layer was larger than that in the bulk. The detailed results of the Rutherford backscattering spectrometry measurements on the plasma-treated active layer in the coplanar TFTs are described elsewhere [27]. Unlike TFTs with a bottom gate structure, the TFTs with a top gate structure were exposed to light that had been transmitted through the glass substrate. The light shield layer was moderately designed to reduce the negative bias temperature illumination stress. The drain current of the TFTs was observed to increase due to a decrease in the drain-induced barrier lowering. Moreover, coplanar TFTs capped with a light shield layer are considered to be superior candidates for use as TFTs with a backplane structure for enhancing the image density of OLEDs. While the reliability of the TFTs with an ESL structure is better than that of the TFTs with a coplanar structure, which is due to the existence of the ESL protecting the active channel layer [28, 29], the parasitic capacitance of the TFTs with an ESL structure is larger than that of the TFTs with a coplanar structure due to the existence of the overlapping area. Furthermore, the photomask number of the coplanar TFTs is smaller than that of the ESL-type TFTs, resulting in a simpler process.

Figure 2 shows that the uniformities of ΔV_{th} , which is the difference between the maximum and the minimum values of the V_{th} for a TFT fabricated on a 2500 mm \times 2200 mm glass, were 0.57 and 0.55 V as determined by using the in-line probe station and the automatic V_{th} sensing method, respectively. This improvement in the uniformity of the V_{th} for the coplanar TFTs, as compared to that of the ESL TFTs, was achieved via the optimization process.

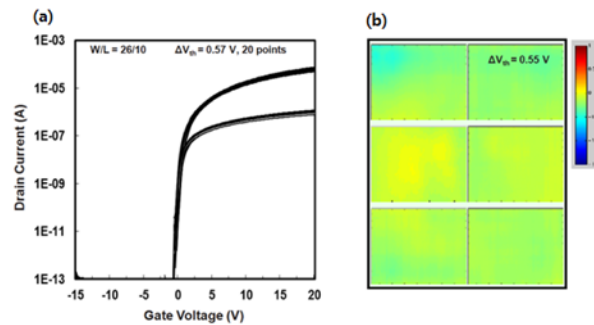


Fig. 2. (a) Drain current as a function of the gate voltage and (b) threshold voltage uniformity for the a-In-Ga-Zn-O thin-film transistors.

Figure 3 shows the drain current as a function of the drain-source voltage (V_{ds}) for various values of the gate-source (V_{gs}) voltage ranging from 5 to 20 V. The variation in the output drain current for the TFTs at $V_{ds} = 10$ V can be characterized by using the differential dI_{ds}/dV_{ds} . The value of that differential in the saturation region for coplanar TFTs with a light shield is almost the same as its value in that region for etch stopper TFTs, indicating that the output current of the OLEDs is not significantly affected by variations in the drain-source voltage.

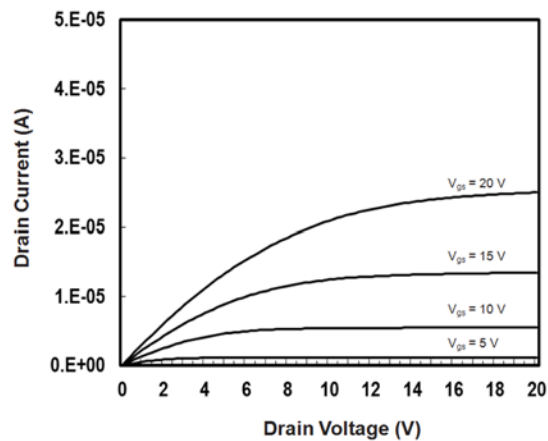


Fig. 3. Drain current as a function of the drain voltage for the a-In-Ga-Zn-O thin-film transistors for different values of the gate voltage V_{gs} .

The shifts in the values of V_{th} for the TFTs were measured under a positive bias temperature stress (PBTS) and under a current stress (CS). Both of these electrical stresses were applied to the TFTs at 60°C using $V_{gs} = +30$ V, $V_{ds} = 0$ V, and a constant current. The shift in the value of V_{th} under the PBTS was 0.07 V after 1 h, as shown in Fig. 4(a), whereas the shift in that value under the CS was 0.03 V after 10 h, as shown in Fig. 4(b). Because the device characteristics of coplanar TFTs vary only slightly during long-time operation, under applied voltages, and exposure to environmental temperatures, such TFTs can be used in large-size OLEDs. The uniformity of the current applied to the TFTs in OLEDs is particularly important if reliable outputs from the OLEDs are to be achieved.

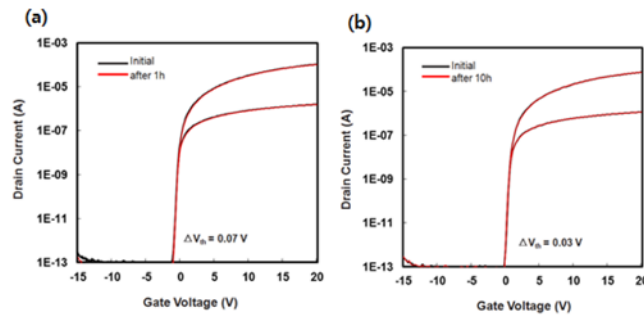


Fig. 4. Drain currents as functions of the gate voltage for the a-In-Ga-Zn-O thin-film transistors with and without (a) a positive gate bias stress at 60°C for 1 h and (b) a current stress at 60°C for 10 h.

Figure 5 shows a cross-sectional view of a large-size OLED embedded with coplanar oxide TFTs fabricated on a $2500 \times 2200 \text{ mm}^2$ glass substrate. The large-size OLED fabricated on 0.5 t glass, which acts as a bottom emission-type display, consists of coplanar-type TFTs, a white OLED (WOLED) with white, red, green, and blue color layers, and the metal encapsulation. Because the emission region of an OLED increases with decreasing size of the TFT, a coplanar TFT with a smaller size would be useful if promising applications in large-size OLEDs are to be realized.

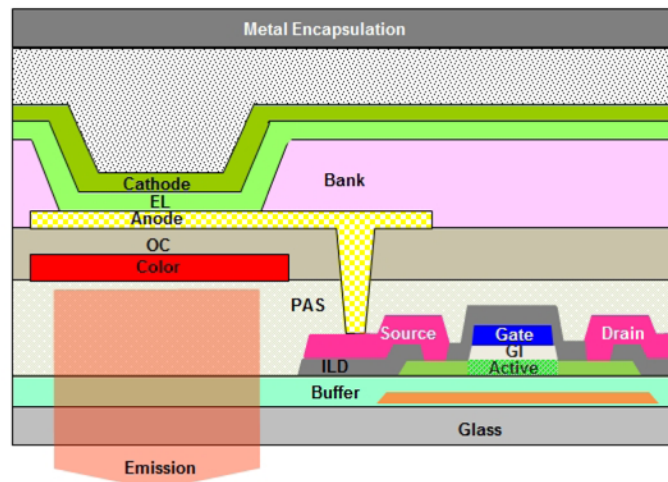


Fig. 5. Cross-sectional view of an organic light-emitting device embedded with an a-In-Ga-Zn-O thin-film transistor with a coplanar structure.

The characteristics of the white OLEDs are summarized in Table 1. The luminance efficiency of the OLEDs at an operating voltage of 11.6 V was 85.0 cd/A. The Commission Internationale de l'Eclairage (CIE) coordinates of the OLEDs are (0.287, 0.310), indicative of a white color, and the dependence of the color shift on the area is only 0.011. The device characteristics of a 55-inch UHID OLED embedded with TFTs with a coplanar structure for practical mass production are summarized in Table 2. One pixel was designed to contain one white, one red, one green, and one blue sub-pixel and to have an average aperture ratio of 30% and a peak luminance of 500 cd/m², thus demonstrating the achievement of an UHID large-size OLED. Although a 55-inch full high-definition OLED panel can be designed using conventional TFTs, 55-inch ultra-high-definition (UHD) panels cannot, which is the reason TFTs with a coplanar structure should be used for the fabrication of UHID large-size OLEDs.

Table 1. Device characteristics of the fabricated OLEDs

Characteristic (Unit)	Value
Voltage (V)	11.6
Efficiency (cd/A)	85.0
Color (W_x, W_y)	(0.287, 0.310)
Color shift ($\Delta u'v'$)	0.011

Table 2. Device characteristics of the 55-inch UHID OLEDs

Characteristic (Unit)	Value
Display type	RGBW OLED
Panel size (inch)	55
Resolution	3840 × 2160 (UHD)
Aperture ratio (%)	30
Brightness (cd/m ²)	150 (full)/500 (peak)
Color gamut (%)	118 (BT. 709)
Contrast ratio	> 1,000,000: 1

Figure 6(a) shows that the maximum luminance of the large-size OLED is 500 nits, indicative of a UHID large-size OLED. As Fig. 6(b) shows, the color gamut of the fabricated OLED satisfies the requirements of the digital cinema initiatives (DCI) of 99%.

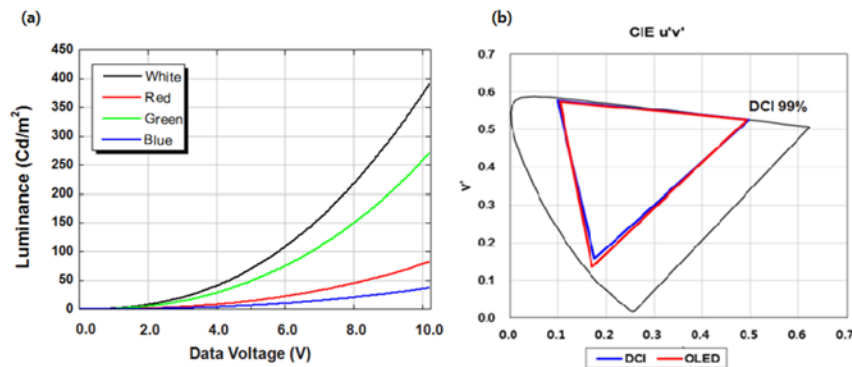


Fig. 6. (a) Current density - voltage, (b) luminance - voltage, (c) current efficiency - luminance characteristics, and (d) normalized electroluminescence spectra of the green and blue OLEDs with a poly-TPD layer and a poly-TPD:DDT-Au nanocomposite layer.

4. Summary and conclusions

The top gate, the self-aligned metallization of the active layer as in the source/drain regions, and the light shield layer of the TFTs were selected so as to enhance the image density of the OLEDs. The a-IGZO oxide TFTs with a coplanar structure on glass substrates showed maximum V_{th} differences of 0.57 V in the TEG transistors and of 0.55 V in the active-area transistors, indicative of their excellent uniformity. The values of the V_{th} for the TFTs with a coplanar structure after having applied a PBTS for 1 h and a CS for 10 h were slightly shifted to 0.07 and 0.03 V, respectively, indicative of their stability. The maximum luminance of the OLEDs embedded with TFTs with a coplanar structure was as large as 500 nits, and their color gamut exhibited a DCI of 99%, indicative of the achievement of large-size UHID OLEDs. The CIE coordinates of the OLEDs were (0.287, 0.310), indicative of a white color, and the dependence of the color shift on the area was only 0.011. Moreover, the luminance efficiency of the white OLEDs embedded with TFTs with a coplanar structure at an operating

voltage of 11.6 V was 85.0 cd/A. Thus, the present observations provide good motivation for envisioning the use of UHID large-size OLEDs embedded with TFTs with a coplanar structure in UHID large-size OLED televisions.

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