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An Improved Single-Phase Full-Bridge ZVS Inverter with a Subtractive Coupled Magnetics

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Abstract – An improved single-phase full-bridge zero-voltage-switching inverter using a subtractive coupled magnetics is proposed in this paper. The proposed topology overcomes several drawbacks of the conventional ARCPI zero-voltage-switching inverter including two bulky capacitors which can cause problems such as the need for a protection circuit and voltage fluctuation of split capacitors. Also the proposed topology can reduce the number of devices required for ZVS through a simplified auxiliary circuit, thus achieving low cost and small volume and is applicable a modified unipolar PWM scheme. Detail mode analysis and design considerations are provided for optimal efficiency. In the end, the effectiveness and feasibility of the proposed topology are verified experimentally under various conditions.

Keywords: Soft-switching, Full-bridge inverter, Modified unipolar PWM scheme, Zero-Voltage-Switching (ZVS), Coupled magnetics

1. Introduction

In general, pulse-width-modulation (PWM) inverters based on a voltage source have been widely employed in various industrial applications such as a power supply, photovoltaic system, energy storage system, variable motor speed drive [1]. In the ideal case, most pulse-width-modulation (PWM) inverters based on a voltage source operate with a high switching frequency as possible in order to improve performance characteristics such as volume, weight, and dynamic response. However, in the practical system, high switching frequency above typically a few hundred kHz naturally induces several problems such as large switching loss and electromagnetic interference (EMI) caused by di/dt and dv/dt. One of the ways to improve the above mentioned problems is the soft switching method using electrical resonance phenomenon through auxiliary resonant passive components and driving an auxiliary device in the auxiliary circuit.

In the past, various methods using soft switching technology have been proposed [2-17], and they can be substantially classified into resonant DC link inverters (RLI) and auxiliary commutated resonant snubber inverters (ACRSI). The RLI has a simple auxiliary circuit and has been applied to various applications; however, it has a problem of device breakdown due to high voltage and high current stress [2]. Additionally, sinusoidal pulse-width modulation (SPWM) schemes are difficult to apply directly.

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The ACRSI, on the other hand, improves these problems through various methods. The ACRSI is divided into several categories such as an auxiliary resonant commutated pole inverter (ARCPI), a zero-voltage transition (ZVT) inverter, and a resonant snubber inverter (RSI) [3]. The ARCPI has the advantages of small rated auxiliary circuitry, but requires two bulky split capacitors which can cause some problems such as voltage fluctuation and balance issues [4, 5]. To avoid the use of split capacitors which can cause the aforementioned problems, various ZVT inverters using coupled inductors have proposed. But the used coupled inductors have some problems such as saturation or volume [7-14]. The RSI overcomes problems related to the two split capacitor, but has the difficulty of applying commonly used modulation schemes such as SPWM or space vector modulation(SVPWM) [15-17]. Consequentially, while the ACRSI is attractive because of low current and voltage stress, it is still subject to other problem such as the requirement of its own auxiliary resonant circuit for each switching leg of the main circuit. For instance, two auxiliary resonant parts are required for a full-bridge circuit, and many auxiliary switches and passive components are needed for ZVS of a full-bridge inverter. Many auxiliary components lead to an increase in volume and cost.

To improve this problem, several modifications of the ARCPI topology are proposed in references [18-20]. Only one auxiliary resonant circuit is required for a full-bridge circuit using the modified ARCPI topology. Additionally, a modified SPWM to enable unipolar switching operation is also introduced to obtain a good output waveform with fewer harmonics. These circuits have similar problems to those mentioned above because it is structurally similar to the existing ARCPI circuit: two bulky split capacitors that cause voltage fluctuation or balance issues, the need for a

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protection circuit to address peak resonant current, extra sensor circuits for voltage balancing of the two split capacitors.

In this paper, an improved single-phase zero-voltage-switching full-bridge inverter using one coupled magnetic with subtractive polarity is proposed. The proposed circuit was inspired by the ZVT inverter circuit, and improve some problems of the existing soft-switching inverter including two bulky spilt capacitors and its protection circuit.

Additionally, based on the magnetic coupling of the coupled magnetic, the proposed circuit can reduce the number of necessary devices via one auxiliary resonant part for a main full-bridge circuit, and thus achieves low cost and small size compared to existing circuits relatively. Moreover, the proposed circuit is applicable a modified SPWM with unipolar operation. In other words, the circuit have advantage such as low harmonics than bipolar switching. Detailed mode analysis and design considerations are provided for optimal efficiency. In the end, the effectiveness and feasibility of the proposed topology are verified experimentally under various conditions.

2. Proposed ZVS Full-Bridge Inverter

2.1 Circuit description

Fig. 1 shows a circuit structure of proposed ZVS inverter. As shown, the proposed circuit can be divided into a main full-bridge inverter for basic inverter operation and auxiliary circuit part for ZVS of main switches.

The proposed circuit consists of four switches, S_1, S_2, S_3, and S_4, their freewheeling diodes, D_1, D_2, D_3, and D_4. Each switches have auxiliary resonant capacitors C_{r1}, C_{r2}, C_{r3}, and C_{r4} for ZVS operation mains switches, S_1, S_2, S_3, and S_4. The additional connected auxiliary resonant circuit for ZVS operation of the full-bridge inverter is consists of two auxiliary switches, S_{a1}, S_{a2}, two auxiliary diodes, D_{a1}, D_{a2}, and one coupled magnetic with subtractive polarity. Note that the auxiliary switches and diodes have a lower rating than the main devices for general inverter operation. The turn ratio N of the coupled magnetic with subtractive polarity combined between the main switch part and the auxiliary switch part is value greater than 1 ($N = N_1 / N_2 > 1$), where the N_1 is the number of turns in the primary winding and N_2 is the number of turns in the secondary winding. L_{r1}, L_{r2} and L_m are primary leakage inductance, secondary leakage inductance and magnetizing inductance of the coupled magnetic.

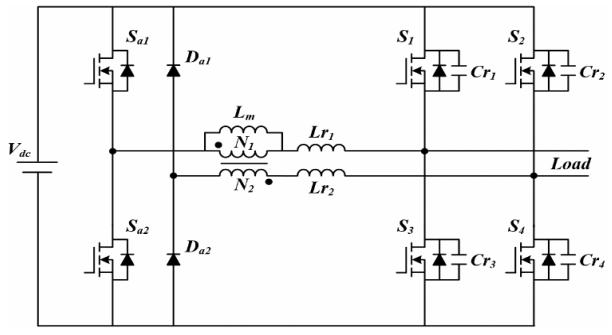


Fig. 1. The circuit diagram of the proposed circuit

The proposed circuit has some merits because of its special shape. First, the circuit can perform zero-voltage-switching of the main switches in a widely-ranged operation point without extra components or circuitry because the turn ratio N of the coupled magnetic is non-unity turns ratio. The non-unity turn ratio of the coupled magnetic makes (N_2/1+N_2) V_{dc} voltage across the leakage inductance L_{r2} of secondary side. The adjusted voltage by non-unity turn ratio is needed for the proposed topology to guarantee ZVS operation of main switches a wide operating point, from light to heavy load conditions. Note that in the conventional ZVS circuits employing the ARCPI circuit, the voltage for ZVS operation is restrict to V_{dc}/2 due to the two split capacitors connected in series. Additionally, in the proposed topology, the current or voltage stress of the components can be reduced. The peak value of resonant current flows through the auxiliary resonance path can be suitably handled within the calculated limit value. This avoids the risk of avalanche to the auxiliary components by the excess peak resonant current occasionally found in the conventional ZVS circuits and enables stable ZVS operation of the proposed circuit.

2.2 Modified unipolar PWM strategy

There are two switching methods for driving a general PWM inverter such as unipolar switching and bipolar switching. It is already known that the output waveform of the PWM inverter includes harmonics caused by switching. It is well known that the unipolar switching method generates less harmonics than the bipolar switching method. However, the proposed circuit is not able to use a conventional unipolar PWM method directly, because one of the main switches of full-bridge circuit always operates under a hard-switching condition. Consequently, a MOSFET device which is typically suitable because of its low switching loss and fast switching speed, is not reasonable at the condition. This limitation is due to the reduced number of auxiliary circuits required for ZVS of the main switches.

In order to overcome this issue, a modified unipolar PWM scheme is applied to the proposed circuit. In the modified unipolar PWM scheme, two switching legs of the full-bridge inverter are switched at each other frequencies. The first leg is operated at high switching frequency, while the second leg operates at low switching frequency where the switching is accurately synchronized to direction of the load current. When the direction of load current is positive, both of the main devices, S_1, S_3 operate at high switching frequency, while S_4 maintains the on-state and S_2 the off-

state. When the direction of load current is negative, S_4 is in the off-state and S_2 in the on-state.

2.3 Operating principles of the proposed circuit

Fig. 2 indicates key waveforms of the proposed soft-switching inverter during one switching cycle, and Fig. 3 indicates circuit diagrams during a switching period. In these figures, the direction of the load current is assumed to be positive.

For intuitive and simple the mode analysis of the proposed circuit, some assumptions are needed: (a) all devices in the proposed circuit are ideal, (b) inductance of the output filter is sufficiently large so that the load current is assumed to be a constant for one switching cycle, (c) the voltage of the dc link capacitor is not variable, and (d) the self-inductance of the coupled magnetic is sufficiently large like an ideal transformer. The fo llowing is a detailed operational analysis of the proposed circuit

Stage 1 [$t < t_0$] – this stage is initial condition. S_4 is in the on-state and S_2 is in the off-state, as shown in Fig. 2. The load current flows through D_3 and S_4, as shown in Fig. 3 (a). Because of D_3 conduction, S_3 is zero-current turned off at the end of Stage 1.

Stage 2 [$t_0 < t < t_1$] – the stage 2 starts when the auxiliary device, $S_{a1,}$ is softly turned on at t_0. Because of to the turn ratio of the coupled magnetic, N, the voltage across the primary resonant inductor, V_{Lr1}, is kV_{dc}, and thus the resonant current, i_{Lr1}, shown Fig. 2 increases linearly in (1). The k represents a conversion coefficient to convert the voltage across the coupled magnetic of the secondary side into the one of the primary. The rising time, t_{01}, is shown in (2).

$$k \cdot V_{dc} = L_{r1}\frac{di}{dt} \text{ where } k = \frac{N^2}{1+N^2} \geq \frac{1}{2}$$
$$i_{Lr1} = i_{load} \text{ where } i_{Lr1} = k \cdot V_{dc}\frac{(t-t_0)}{L_{r1}} \quad (1)$$

$$t_{01} = \frac{L_{r1} \cdot i_{Lr1}}{k \cdot V_{dc}}. \quad (2)$$

Stage 3 [$t_1 < t < t_2$] – the stage 3 starts when the i_{Lr1} becomes i_{load} at t_1. The resonance between the auxiliary inductor, L_{r1}, and the auxiliary capacitors, C_{r1} and C_{r3}, begins as shown in Fig. 3 (c). The resonance is continued for this section, t_{12}. When C_{r1} is completely discharged and C_{r3} is charged relatively, i_{Lr1} reaches its peak value, i_{Lr1_peak}. The resonant peak current, i_{Lr1_peak}, the resonant angular frequency, ω_r, the resonant period, T_r, and the combined impedance, Z_r can be shown in (3). The resonance time, $t_{12,}$ is expressed in (4),

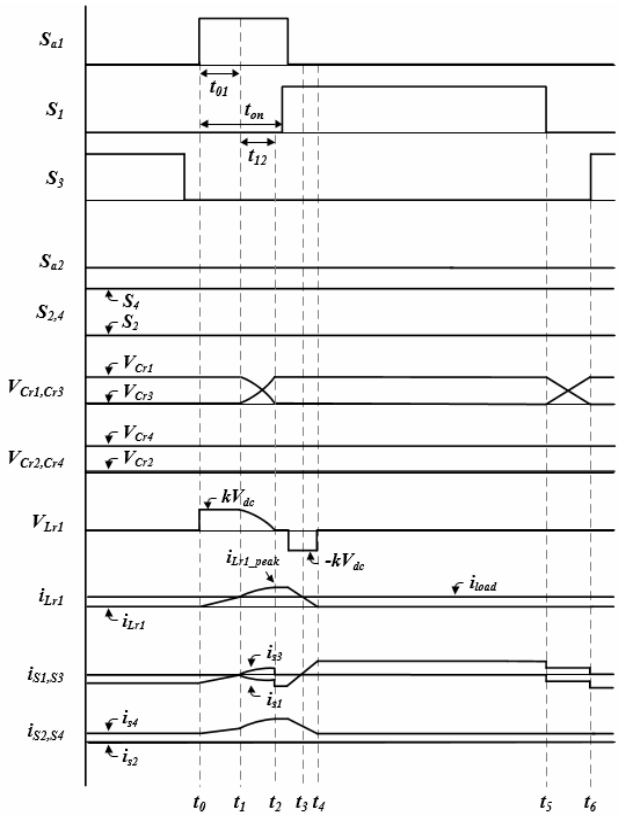


Fig. 2. Key waveforms for a switching period under at positive load current

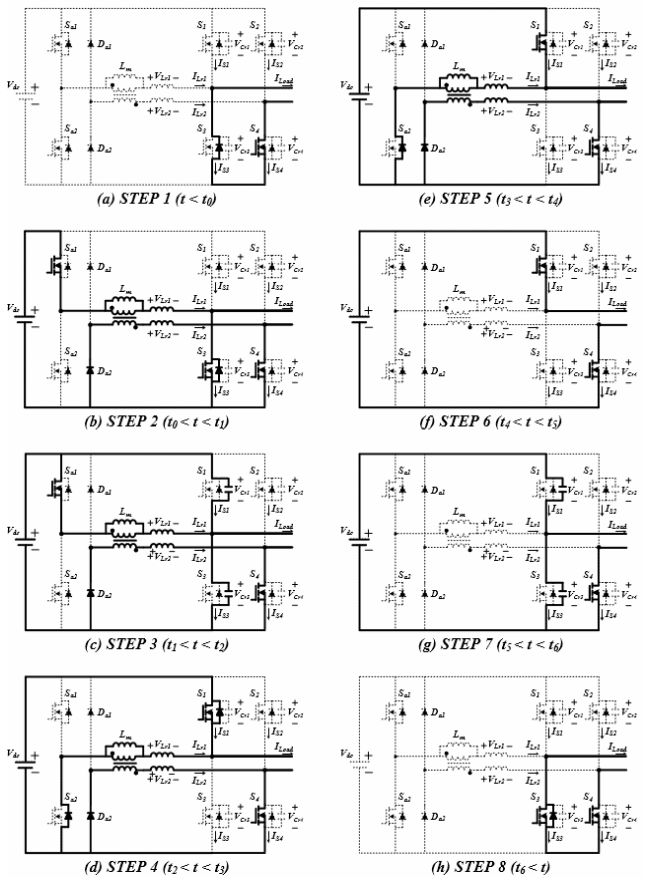


Fig. 3. Circuit diagrams for a switching period at positive load current

$$i_{Lr_peak} = \frac{V_{cr}(t_1)}{Z_r}\sin(\frac{1}{4}T_r) + i_{Lr1}(t_1)$$
$$\omega_r = \frac{1}{\sqrt{2C_r \cdot L_{r1}}} \text{ where } Z_r = \sqrt{\frac{L_{r1}}{2C_r}}, \quad (3)$$

$$t_{12} = \frac{2\pi\sqrt{2C_r \cdot L_{r1}}}{4} = \frac{\pi\sqrt{2C_r \cdot L_{r1}}}{2}. \quad (4)$$

Stage 4 [$t_2 < t < t_3$] – the stage 4 starts when the resonance between L_{r1} and C_{r1}, C_{r2} is finished at t_2. Since the voltage, V_{Cr1}, is zero, D_1 starts to conduct resonant current. S_1 is turned on at a ZVS state. S_{a1} is turned off so that the voltage across the primary auxiliary resonant magnetic, V_{Lr1}, becomes $-kV_{dc}$. The current i_{Lr1} is reduced linearly and the current i_{S1} of the switch S_1, is increased as expressed in Fig. 2. In order to guarantee a ZVS operation, S_1 should be turned-on after time t_{02} as shown in Eq. (5),

$$t_{on} \geq t_{01} + t_{12} = \frac{L_{r1} \cdot i_{Lr1}}{k \cdot V_{dc}} + \frac{\pi\sqrt{2C_r \cdot L_{r1}}}{2} \quad (5)$$

Stage 5 [$t_3 < t < t_4$] – the stage 5 begins when the i_{Lr1} is smaller than the i_{load} at the t_3. The direction of the i_{S1} is changed from negative to positive, and it causes to blocking the freewheeling diode D_1 as expressed in Fig. 3 (e). The S_1 begins to conduct and the current i_{S1} of the main switch S_1 keeps rising linearly. The i_{Lr1} keeps falling until it becomes zero as shown in Fig. 2.

Stage 6 [$t_4 < t < t_5$] – the stage 6 begins when the voltage, V_{Lr1}, becomes zero at t_4. This stage is the same as the operation of the ordinary full-bridge inverter. S_1 and S_4 are in the on-state and carry the full load current, as shown in Fig. 3 (f).

Stage 7 [$t_5 < t < t_6$] – the stage 7 starts when S_1 is turned off at t_5. The voltage of C_{r1} is linearly charged and the voltage of C_{r3} is linearly discharged relatively because of to the constant load current, as shown in Fig. 2.

Stage 8 [$t_6 < t$] – this interval is equal to dead time of the typical inverter. The stage 8 starts when S_3 is turned on under a ZVS condition without operation of the auxiliary switches because voltage of the C_{r3} is discharged at the previous stage, as shown in Fig. 3 (h).

3. Design Consideration

3.1 Turn ratio N of the coupled magnetic

Eq. (1) describes the load current ratio where the voltage of the dc-link capacitor has a important role. Assuming the voltage of the dc-link capacitor is the same, a larger load current needs a larger k to fulfill a ZVS of the main switches. By obtaining a fully large k, dependency decreases on the source and load variations and thus this makes ZVS operation possible over a wider range [10]. In this design, $k > 0.5$ is proposed where the coupled magnetic turn ratio, N, is shown in (6),

$$k = \frac{N^2}{1+N^2} \geq \frac{1}{2}. \quad (6)$$

Considering the damping effect and losses which occur for the resonance period, it needs the system to be slightly altered to (7) where Q ($= \omega_r L_r / R$) is the resonance qualification factor and R is the equivalent resistance of the resonance path [9-11],

$$\frac{N^2}{1+N^2} - \frac{R \cdot \pi}{8 \cdot \omega_r \cdot L_r} \geq \frac{1}{2}. \quad (7)$$

Finally, Eq. (7) can be clearly simplified as shown in (8),

$$N \geq \sqrt{\frac{4Q+\pi}{4Q-\pi}}. \quad (8)$$

The coupled magnetic turn ratio N needs to be minimized to decrease its size as long as Eq. (8) is satisfied. In this paper, N is selected to 1.2 and k to 0.59.

3.2 Resonant capacitance

In order to reduce turn-off loss of the main switch, the resonant capacitance, C_r, needs to be optimized. C_r affects dv/dt and turn-off loss P_{OFF} of the device [11]. These are described as (9) and (10) where I_{load} is the load current, t_f is the component's turn-off fall time, and T_{SW} is the PWM period:

$$P_{OFF} = \frac{1}{3}\frac{(I_{load} \cdot t_f)^2}{24 \cdot C_r \cdot T_{SW}} \quad (9)$$

$$\frac{dv}{dt} = \frac{I_{load}}{2 \cdot C_r}. \quad (10)$$

In this paper, the resonant capacitances C_{r1}, C_{r2}, C_{r3}, and C_{r4} are set to 10 nF based on several experimental tests which were performed using a reasonable trade-off of the P_{OFF} and the dv/dt in the main switches.

3.3 Resonant Inductance

The value of the auxiliary inductance is also a trade-off between di/dt and loss of the auxiliary device. A large value of the auxiliary inductance causes to a gradual di/dt, yet increases the conduction loss of the auxiliary device. It is proposed in order to obtain a appropriate di/dt, values ranging from 10 A/μs and 50 A/μs should be chose as.

$$10A/\mu s \leq \frac{di}{dt} = k\frac{V_{dc}}{L_r} \leq 50A/\mu s. \quad (11)$$

The primary resonant inductance, L_{r1}, is chosen at 17 μH

based on some experimental tests and a reasonable trade-off of the *di/dt* and the conduction loss in this paper. The expected *di/dt* is 11 A/μs, which satisfies Eq. (11).

4. Feasibility Verification of the Proposed Circuit

Several experiments were performed in order to verify performance and feasibility of the proposed circuit, where the switching frequency of the main devices, S_1 and S_3, is set to 10 kHz, and that of S_2 and S_4 to 60 Hz. Fig. 4 shows a set of experiments, which were carried out to verify the proposed contents. The experimental set consists of a single-phase inverter, auxiliary circuits, and a DSP board for control. Table 1 shows the circuit parameters applied in the experiment, which are as explained in the previous sections.

Fig. 5 shows the ZVS waveforms of the main devices, S_1 and S_3, at a positive load current and a negative load current condition. When the direction of load current is positive, Fig. 5(a) shows the ZVS operation of the main switches. It is obvious that the voltage of the auxiliary capacitor, V_{Cr1}, drops to zero upon operating the auxiliary device, S_{a1}, before turning on the main switches, S_1 and S_3. As a result, main switches, S_1 and S_3, are turned on at the ZVS condition. The voltage of the resonant capacitor, V_{Cr3}, drops to zero by operating the auxiliary switches. When the direction of load current is negative, Fig. 5(b) shows the similar operation, and similar operations can be shown in the main devices, S_1 and S_3.

Fig. 6 shows the output voltage on the load side when the proposed unipolar PWM method is applied under a full

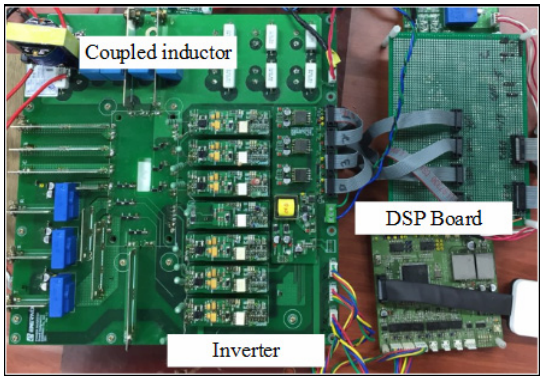
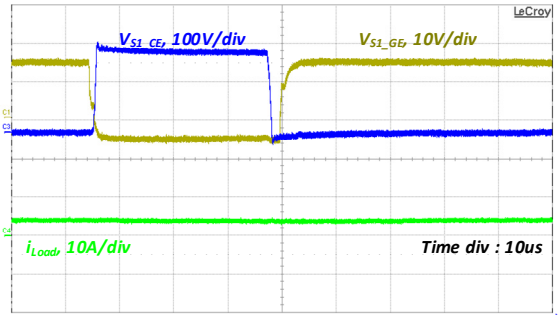
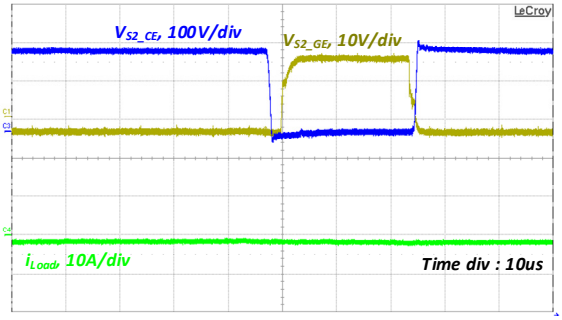


Fig. 4. The prototype 3-phase inverter for the experiment



(a) ZVS waveforms at positive load current state



(b) ZVS waveforms at negative load current state

Fig. 5. ZVS operation waveform according to load current direction

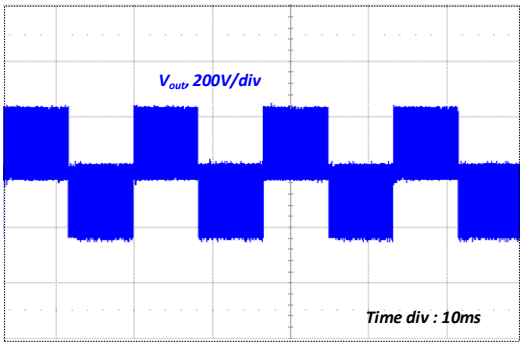
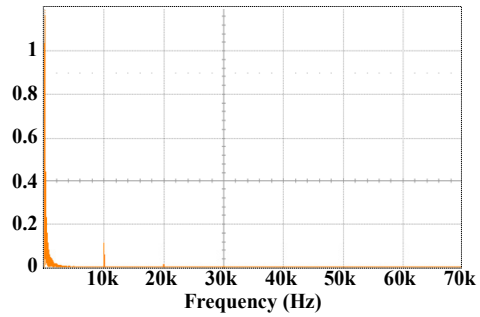
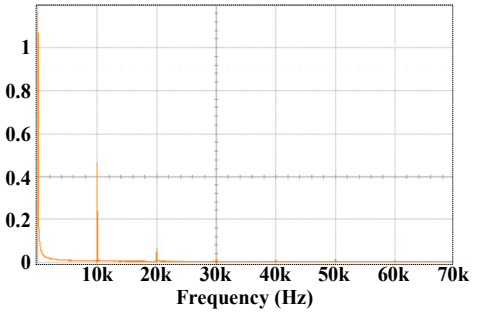


Fig. 6. Waveforms of the output voltage



(a) FFT analysis of the modified unipolar PWM technique



(b) FFT analysis of the basic bipolar PWM technique

Fig. 7. FFT analysis of output current between the modified unipolar PWM and bipolar PWM technique

Table 1. Circuit parameters

Parameters	Value[Unit]
Switching Frequency (f_s)	10 [kHz]
DC Link Voltage (V_{dc})	200 [V]
Resonant Capacitance (C_r)	10 [nF]
Resonant Inductance (L_r)	17 [uH]
Rated Output Power (P_{out})	500 [W]
Output Current (I_{out})	4.2 [A]

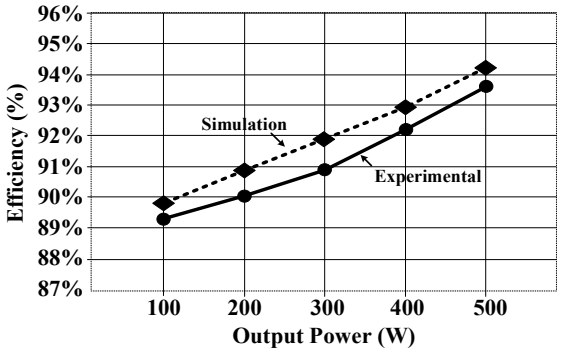


Fig. 8. Efficiency comparison of the simulation and experimental results

load condition of P_{out} = 500 W. The output voltage changes from -V_{dc} to zero for a positive half period of fundamental frequency, or from zero to V_{dc} for a negative half period.

Fig. 7 shows the comparison between the proposed unipolar switching method and the conventional bipolar switching method through FFT analysis. Fig. 7(a) presents the results of the modified unipolar PWM technique and Fig. 7(b) the bipolar PWM technique. As shown, the modified unipolar PWM technique has better performance of the output waveform with less harmonics than the bipolar PWM scheme.

Fig. 8 shows, depending on various output power, the efficiency of the proposed circuit under the condition that the modified unipolar PWM scheme of 10kHz is applied. Since the loss of the coupled magnetic is not reflected in the simulation result, the efficiency of the soft-switching inverter is approximately 0.5% lower than that of the simulation result at a full load condition (P_{out} = 500 W).

5. Conclusion

In this paper, an improved single-phase full-bridge zero-voltage-switching inverter using one coupled magnetics with subtractive polarity is proposed. The proposed circuit is applicable modified unipolar PWM scheme and has only one auxiliary resonant set, which leads to reduced cost and volume. Also, the circuit improves the problems of conventional soft-switching inverter topology such as the requirement of two bulky capacitors, protection circuit, and voltage fluctuation of the split capacitors. The effectiveness and feasibility of the proposed topology was verified by the various experimental results with the values selected through the design procedure.

Acknowledgements

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References

[1] N. Mohan, T.M. Undeland, and W. P. Robbins, "Power Electronics: Converters, Applications and Design," John Wiley and Sons, 1989.

[2] D. M. Divan, "The resonant dc link converter - A new concept in static power conversion," in *Conf Rec. IEEE IAS Annu. Mtg.,* Oct. 1986, pp. 648-656.

[3] Jih-Sheng Lai, "Fundamentals of A New Family of Auxiliary Resonant Snubber Inverters," *IECON 97*, *23rd International Conference on Industrial Electronics*, *Control and Instrumentation*, pp. 645-650, 1997.

[4] R. W. De Donker, J. P. Lyons, "The auxiliary resonant commutated pole converter," *IEEE Industry Applications Society Annual Metting Record*, vol. 2, pp. 1228-1235, 1990.

[5] R. W. De Doncker and J. P. Lyons, "The auxiliary quasi-resonant dc link inverter," *Conf. Rec. of IEEE PESC*, pp. 248-253, 1991.

[6] W. McMurray, "Resonant snubbers with auxiliary switches," *IEEE Trans. on Ind*. Appl., vol. 29, no. 2, Mar.lApr. 1993, pp. 355-362.

[7] J. P. Gegner and C. Q. Lee, "Zero-voltage transition converters using inductor feedback technique," *Conf. Rec. of IEEE APEC*, pp. 862-868, 1994.

[8] S. Frame, S. Dubovsky, Q. Li, Katsis, C. Cuadros, D. Borojevic and F. C. Lee, "Three-phase soft-switching inverters for electric vehicle applications," *Proc. of 1995 VPEC Seminar*, pp. 45-52, 1995

[9] V. Vlatovic, D. Borojevic, F. C. Lee, C. Cuadros and S. Gataric, "A new zero-voltage transition, three-phase PWM rectifier/inverter circuit," *Conf. Rec. of IEEE PESC*, pp. 868-873, 1993.

[10] X. Yuan and I. Barbi, "Analysis, designing, and experimentation of a transformer-assisted PWM zero-voltage switching pole inverter," *IEEE Trans. Power Electron.*, vol. 15, no. 1, pp. 72-82, Jan. 2000.

[11] W. Yu, J. Lai and S. Park, "An improved zero-voltage switching inverter using two coupled magnetics in one resonant pole," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 952-961, 2010.

[12] L. Jiang, C. C. Mi, S. Li, C. Yin and J. Li, "An Improved Soft-Switching Buck Converter With Coupled Inductor," *IEEE trans. on Power electronics*, vol. 28, no. 11, pp.4885-4891, 2013.

[13] J Lai, J Zhang and H Yu, "Source and Load Adaptive Design for a High-Power Soft-Switching Inverter," *IEEE Trans. on Power electronics*, vol. 21, no. 6, pp. 1667-1675, Nov, 2006.
[14] W. Dong, D. Peng, H. Yu, F. C. Lee, and J. Lai, "A simplified control scheme for zero voltage transition (ZVT) inverter using coupled inductors," *Proc. IEEE Power Electron. Spec. Conf.*, pp. 1221-1226, 2000.
[15] J. S. Lai, R. W. Young, G. W. Ott, C. P. White, J. W. McKeever and D. S. Chen, "A novel resonant snubber based soft-switching inverter," *Conf. Rec. of IEEE APEC*, pp. 797-803, 1995.
[16] J. S. Lai, R. W. Young, G. W. Ott, J. W. McKeever and F. Z. Peng, "A delta configured auxiliary resonant snubber inverter," *IEEE Trans. on Ind. Appl.*, vol. 32, no. 3, pp. 518-525, 1996.
[17] Jih-Sheng Lai, "Resonant snubber based soft-switching inverters for electric propulsion drives," *Industrial Electronics, Control, and Instrumentation, 1996.*, *Proceedings of the 1996 IEEE IECON 22nd International Conference on*, vol. 1, pp. 47-52, 5-10 Aug. 1996.
[18] Moah-Chin Jiang; Wei-Shiang Wang; Huang-Kai Fu; Kuei Wu-Chang; Min-Lun Tsai; Kao-Ui Lu, "A Novel Single-Phase Soft-Switching Unipolar PWM rectifier," *TECON 2011-2011 IEEE Region 10 Conference*, pp.843-847, 2011.
[19] Moah-Chin Jiang; Chien-Ming Wang; Shyh-Shing Perng, "A Novel Single-Phase Soft-Switching Unipolar PWM Inverter," *Proc. 8th Int. Conference Power Electronics*, *ECCE Asia*, pp. 2874-2879, 2011.
[20] Moah-Chin Jiang; Wei-Shiang Wang; Huang-Kai Fu; Kuei Wu-Chang; Huang-Kai Fu; Min-Lun Tsai; Kao-Ui Lu, "A Novel Single-Phase Soft-Switching Unipolar PWM Shunt Active Power Filter," *in Industrial Electronics and Application*, *2012 8th IEEE Conference on*, pp.2081-2086, 2012.

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