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RESEARCH ARTICLE

High-Powered RF SOI Switch With Fast Switching Time for TDD Mobile Applications

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ABSTRACT This paper presents a fast switching and high-powered single-pole double-throw (SPDT) switch for RF switch circuits, such as TRx antenna switches and frequency band (or operation mode) selection switches in mobile handset applications. For fast switching time and performances of the RF switch, we proposed a novel method that can ''selectively'' control the impedance of a gate biasing circuit (''high'' or ''low'' impedance). The proposed SPDT switch use the low impedance of the gate biasing circuit for fast switching time and use the high impedance of the gate biasing circuit to avoid the degradation of the insertion loss and harmonics. The proposed SPDT switch has no additional bias and no large payment for size consumption. According to measurement results, the turn-on switching time of the proposed SPDT switch was 0.35 μs (at 2 GHz). The insertion loss, isolation, and return loss at 2 GHz were 0.16 dB, 47.1 dB, and 24 dB respectively. 2nd and 3rd harmonic levels at 25 dBm input power at 2 GHz were −88.7 dBm and −78.9 dBm, respectively. Power handling capability was 39.5 dBm of input power at 2 GHz. The designed SPDT switch was implemented in a 0.13-μm partially depleted silicon-on-insulator (PD-SOI) process.

INDEX TERMS Fast switching time, high-power handling, partially depleted silicon-on-insulator (PD-SOI), RF switch, single-pole double-throw (SPDT).

I. INTRODUCTION

The time division duplexing (TDD) technique has been used since the introduction of long-term evolution (LTE), including in the 5th-generation (5G) mobile communication. Because TDD uses the spectrum more flexibly than frequency division duplexing (FDD) and is better suited to burst traffic demands, TDD has become a more attractive duplexing method than FDD. But to deliver even one round trip transmission of a control signal or a data signal, several uplink (UL) and downlink (DL) cycles are required in the TDD system. This leads to the requirement of fast and flexible link direction switching [1]. UL and DL switching guard times are limited by the interface latency and Tx/Rx switching time. Thus, the importance of the switching time of the antenna switches is increasing.

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As the switching time of the antenna switch becomes important, methods for improving the switching time have been proposed. To reduce the switching time, reference [2] and [3] proposed the methods that are optimizing or using complex analog circuits with the reduced gate biasing resistors. Reference [2] optimized the transistor size of the logic driver and reduced the gate biasing resistors. For fast switching time, reference [3] used high operating voltage of ''3 V'' that is higher than the supplied voltage of 1.8 V. But, to make high operating voltage of 3 V, a low dropout (LDO) circuit and a charge pump circuit should be added inevitably. And reference [3] also used the reduced gate biasing resistors for the purpose simultaneously. Since these both methods reduced the gate biasing resistors for fast switching time, however, the insertion loss and 2nd harmonic are unfortunately degraded accordingly.

Therefore, in this work, to avoid the performance degradation of the insertion loss and 2nd harmonic, we proposed

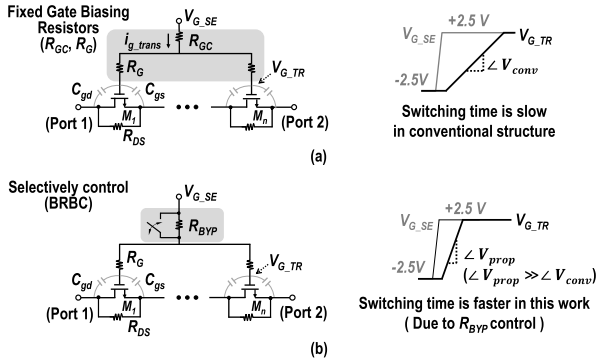

FIGURE 1. (a) The conventional and (b) the proposed structures of the series branch in the SPDT switch.

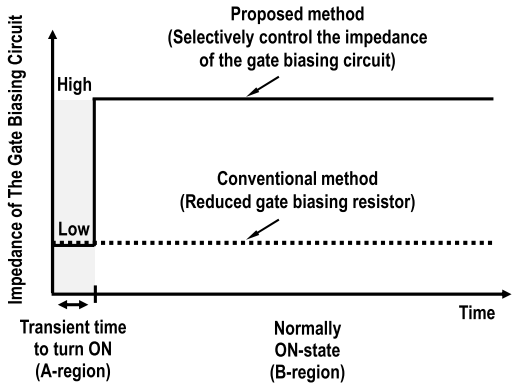

FIGURE 2. The time diagram about the impedances of both conventional method that have been using the reduced gate biasing resistors and proposed method that selectively control the impedance of the gate biasing circuit.

a novel method that can ''selectively'' control the impedance of a gate biasing circuit (''high'' or ''low'' impedance). Fig. 1 shows a conventional structure with fixed gate biasing resistors (Fig. 1(a)), and the proposed structure with the selective control of gate biasing circuit (Fig. 1(b)). The time diagram about the impedances of the conventional method which has been using the ''low'' gate biasing resistors and the proposed method which ''selectively'' control the impedance of the gate biasing circuit is described in Fig. 2. For fast switching time, the biasing resistor bypass circuit (BRBC) in the Fig. 1(b) is turned ''ON'' to reduce the impedance of the gate biasing circuit just during the transient time which means the time duration between when the control signal reached 50 % of its final value and when the output signal reached 90 % of its target maximum RF peak value (A-region in Fig. 2). And then, BRBC is turned ''OFF'' to make ''high'' impedance of the gate biasing circuit during normally ON-state of the RF switch (B-region in Fig. 2), so the proposed RF switch can be implemented without any performance degradation of the insertion loss and 2nd harmonic. Thus, the proposed method is suitable for applications such as high-power user equipment (HPUE) and multi-band antenna switches.

This paper is organized as follows. In Section II, we introduce the main factors affecting the switching time of typical

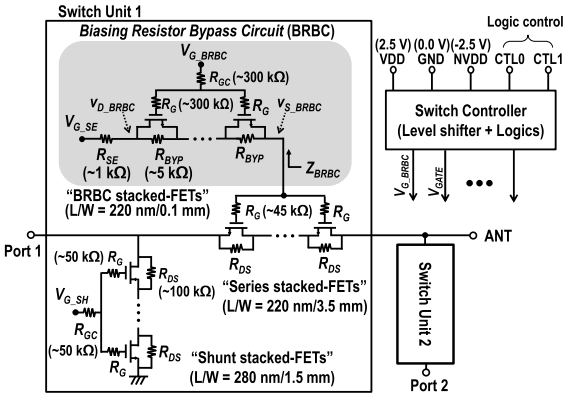

FIGURE 3. Simplified schematic of the proposed SPDT switch with a BRBC.

RF switches and the design concepts of the fast switching and high-power handling method of the proposed SPDT switch. The simulation results, the measurement setup and the implemented measurement results are presented in Section III. And Section IV concludes this paper.

II. DESIGN CONCEPT

A. SWITCHING TIME ANALYSIS OF TYPICAL HIGH-POWER RF SWITCH

As shown in Fig. 1(a), the conventional structure has been used a floating gate/body [4], negative biasing [5], and stacked-FET [6], [7], [8]. However, to handle a high-power while using conventional structure, these techniques use large value gate resistors (R_G) and common gate resistor (R_{GC}). These resistors slow down the voltage charging and discharging time by limiting the transient current (i_{g_trans}). Also, transistors with wide total gate width used to improve the insertion loss slow down the voltage charging and discharging time by large value parasitic capacitors such as gate-source capacitors (C_{gs}) and gate-drain capacitors (C_{gd}) [8]. If transistors are replaced by parasitic capacitors (C_{gs}, C_{gd}) as shown in Fig. 1(a), this circuit is a kind of the RC charging/discharging circuit.

Thus, there are two methods to control the switching time: one is to control the biasing resistors and the other is to control the size of the transistors. In this paper, R_{GC} which affects all the stacked-FETs, was selectively controlled by the proposed biasing resistor bypass circuit (BRBC) as shown in Fig. 1(b).

B. DESIGN STRUCTURE OF THE BRBC

Typically, to reduce the insertion loss, wide transistors have been used in the series branch. And since wide transistors cause the large parasitic capacitances (C_{gs}, C_{gd}), the series branch represents the dominant part of the switching time. As shown in Fig. 3, to control the dominant part of switching time, the BRBC is only implemented in the series branch of the SPDT switch. To improve the switching time of the BRBC, the BRBC is designed with narrow total gate width transistors. And since the BRBC has to handle the RF peak voltage that are induced from the RF signal path, BRBC

TABLE 1. Operating DC bias in BRBC.

DC BIAS	TURNING ON (A-REGION)	NORMALLY ON (B-REGION)	TURNING OFF (C-REGION)	NORMALLY OFF (D-REGION)
V_{G_SE} (V)	2.5	2.5	−2.5	−2.5
V_{G_BRBC} (V)	2.5	0	2.5	0
V_{B_BRBC} (V)	0	0	−2.5	−2.5
STATE OF BRBC	ON-STATE	OFF-STATE	ON-STATE	ON-STATE

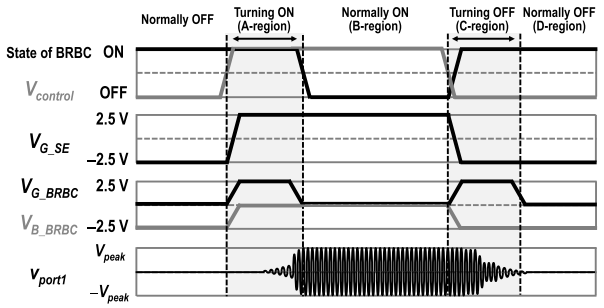

FIGURE 4. Time diagram of DC bias in the BRBC and transient voltage of port 1.

is designed with 8 stacks transistors. To decrease the RF signal leakage, when the BRBC is OFF-state, 5 kΩ bypass resistors (R_{BYP}) are used for each of the transistors in the BRBC as shown in Fig. 3. A 1 kΩ series resistor (R_{SE}) is also used to decrease the harmonic level and increase the power handling capability. To control the ON-state and OFF-state of the BRBC, a switch controller is designed and integrated into the chip.

C. HIGH-POWER HANDLING AND FAST SWITCHING TIME SCHEME OF BRBC

To briefly explain the fast switching operation of the SPDT switch, when the BRBC is turned on, the impedance of BRBC (Z_{BRBC}) is reduced due to the on-resistances of the transistors in the BRBC. Through this, fast switching time can be achieved. And when the BRBC is turned off, Z_{BRBC} is high impedance due to the R_{BYP} and the off-capacitance of the transistors in the BRBC. This high impedance minimizes the degradation of the insertion loss and 2nd harmonic during the normally ON-state. As shown in Table 1 and Fig. 4, in the A-region, to quickly turn on the RF switch, transistors in the BRBC are turned on with a transistor gate voltage in the BRBC (V_{G_BRBC}) of 2.5 V during the switching time of the SPDT switch. In the B-region, the series branch of the RF switch is ON-state. Thus, the DC voltage of the drain and source of the BRBC's transistors is 2.5 V. For high-power handling capability of the SPDT switch, BRBC also has to handle high RF peak voltage. Thus, negative biasing and OFF-state are applied to the BRBC by the V_{G_BRBC} of 0 V. In the C-region, to quickly turn off the RF switch, transistors in the BRBC are turned on with the V_{G_BRBC} of 2.5 V. In the D-region, the series branch of the RF switch is OFF-state. Thus, the DC voltage of the drain and source of the BRBC's transistors are −2.5 V. The V_{G_BRBC} of −2.5 V can't apply the negative biasing technique and OFF-state for the BRBC simultaneously. Thus, this work uses the ON-state of BRBC with the V_{G_BRBC} of 0 V. And R_{SE} which is significantly higher impedance (1 kΩ) than the on-resistances of the transistors is used in the BRBC as shown in Fig. 3. When the SPDT switch is OFF-state and the BRBC is ON-state, most of the RF peak voltage between the source voltage of the BRBC (v_{S_BRBC}) and the gate voltage of the series branch (V_{G_SE}) is applied not to the transistors in the BRBC but to the R_{SE}. The relationship between the R_{SE}, the number of stacks of BRBC, and RF peak voltage that BRBC has to handle is:

$$BV_{DS} > \frac{v_{sd\_brbc}}{m} = \frac{1}{m} \times \frac{Z_{TR\_BRBC}}{(Z_{TR\_BRBC} + R_{SE})} \times (v_{S\_BRBC} - V_{G\_SE}) \quad [\mathrm{V}] \tag{1}$$

$$R_{SE} > \frac{Z_{TR\_BRBC}}{m \times BV_{DS}} (v_{S\_BRBC} - V_{G\_SE}) - Z_{TR\_BRBC} \quad [\Omega] \tag{2}$$

Here, BV_{DS} represents the unit transistor breakdown voltage between the drain and source, v_{S_BRBC} represents the RF peak voltage with the DC voltage at the source of the BRBC, v_{sd_brbc} (= $v_{S\_BRBC} - v_{D\_BRBC}$) represents the RF peak voltage between source and drain of the BRBC transistors, Z_{TR_BRBC} (= $Z_{BRBC} - R_{SE}$) represents the impedance between the drain and source of the total BRBC transistors, m represents the number of transistor stacks in the BRBC, and V_{G_SE} represents the DC gate biasing voltage of the RF switch. These variables are illustrated in Fig. 3. As shown in (1), increasing the number of transistor stacks (m) in the BRBC and increasing the R_{SE} alleviate the RF peak voltage that the unit transistors in the BRBC has to handle. However, the increased R_{SE} slows down the switching time. Through this and the relationship between the R_{GC} and the switching time which is described in Section II-A, the R_{SE} is consequently the trade-off point between the power handling capability and the switching time.

D. CONVENTIONAL STRUCTURE AND PROPOSED STRUCTURE COMPARISON ACCORDING TO GATE BIASING RESISTANCES

As mentioned in Section II-A, the value of the biasing resistors is the dominant factor of the switching time. And they also affect the insertion loss and 2nd harmonic level of the RF switches. Thus, to compare the conventional structure and proposed structure, these cases are simulated and described in Table 2. Case-0 used biasing resistors of commonly used values, such as R_{GC} of 50 kΩ and the R_G of 50 kΩ. Because of the high value of biasing resistors, intrinsic insertion loss is 0.144 dB, switching time is 1.36 μs, and 2nd harmonic level at 25 dBm input power is −79.7 dBm. Case-1 has a switching time similar to that of the proposed structure with the R_{GC}

TABLE 2. RF switch comparison table according to biasing resistance.

Simulation Results	SPDT			
	Conventional Structure			Proposed Structure
	Case-0 ($R_{GC} \cong 50$ kΩ, $R_G \cong 50$ kΩ)	Case-1 ($R_{GC} \cong 0$ Ω, $R_G \cong 50$ kΩ)	Case-2 ($R_{GC} \cong 0$ Ω, $R_G \cong 10$ kΩ)	
Frequency (GHz)	2.0	2.0	2.0	2.0
Intrinsic Insertion loss (dB)	0.144	0.182	0.342	0.155
Isolation (dB)	46.7	46.7	46.9	46.8
2nd Harmonic# (dBm)	−79.7	−75.2	−52.1	−79.5
3rd Harmonic# (dBm)	−84.1	−84.3	−73.2	−84.1
Turn-on Switching Time* (μs)	1.36	0.34	0.31	0.34

* Time duration between the 50 % of the Vcontrol and the 90 % of the maximum RF peak value
# P_{in} = 25 dBm at 2 GHz

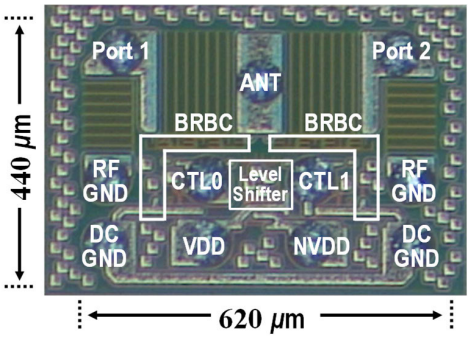

FIGURE 5. Photograph of the proposed SPDT switch.

of 0 Ω and the R_G of the 50 kΩ. Intrinsic insertion loss is 0.182 dB, switching time is 0.34 μs, and 2nd harmonic level at 25 dBm input power is −75.2 dBm. The switching time of Case-1 is faster than Case-0, but the insertion loss and 2nd harmonic level are degraded. Case-2 has much lower values of biasing resistors at the R_{GC} of the 0 Ω and the R_G of the 10 kΩ. Intrinsic insertion loss is 0.343 dB, switching time is 0.31 μs, and 2nd harmonic level at 25 dBm input power is −52.1 dBm. Because the switching time is limited by the shunt branch, switching time is similar to Case-1. But the insertion loss and 2nd harmonic level at 25 dBm input power are more degraded than Case-1. Through this, biasing resistors are one of the dominant trade-off factors between switching time, the insertion loss and 2nd harmonic level. To improve these performances, BRBC structure is proposed. The proposed structure has a switching time similar to Case-1, but the insertion loss is improved 14.8 % and the 2nd harmonic level is improved 5.7 % compared to the conventional Case-1.

III. MEASUREMENT RESULTS AND COMPARISON

The designed SPDT switch was fabricated using the 0.13-μm PD-SOI CMOS process, as shown in Fig. 5. The size

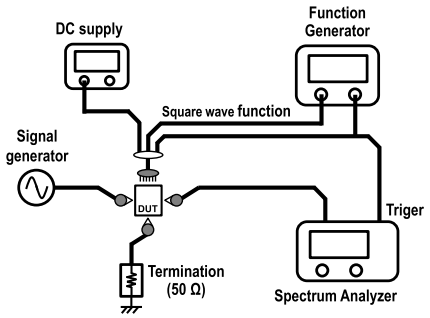

FIGURE 6. Measurement setup of the switching time.

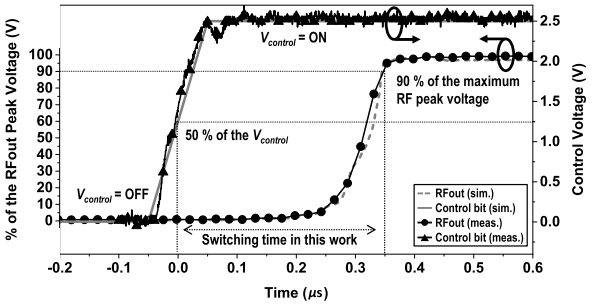

FIGURE 7. Simulation and measurement results of the switching time at a 2 GHz of the RF frequency.

of the additional circuits including the BRBC was 0.010 mm^2 each series branch. All the circuit components which are the RF switch, ESD protection block, level shifter, and proposed BRBC were integrated into a single chip of 620 μm × 440 μm. All measurements were performed using a probe tip on the multi-layer printed circuit board (PCB).

A. SWITCHING TIME

The switching time was simulated and measured at the RF frequency of 2 GHz. As shown in Fig. 6, to iteratively control the ON-state and OFF-state of the SPDT switch, a function generator (Tektronix AFG1022) was used to generate a 50 kHz square wave that varies between 0 V and 2.5 V. This wave function was applied as the control bit of the SPDT switch and to trigger the spectrum analyzer (Keysight PXA-N9030A). Spectrum analyzer measures the RF power to measure the switching time of the SPDT switch. As shown in Fig. 7, the measured RF power was converted to a percentage of the maximum RF peak voltage in the normally ON-state of the SPDT switch. The switching time was defined as time duration between when the control signal reached 50 % of its final value and when the output signal reached 90 % of its target maximum RF peak value [2], [9], [11], [12], [13]. The measured turn-on switching time of the proposed SPDT switch was 0.35 μs. The measurement results follow the simulation results well.

B. S-PARAMETER

The S-parameter of the SPDT switch was measured by the network analyzer (Rohde-Schwarz ZVA50). All the measured

TABLE 3. State-of-the-art SOI CMOS SPDT switches.

References	[2]	[3]	[10]	[11]	[9]	This work
Architecture	SPDT	SPDT	SPDT	SPDT	SPDT	SPDT
Frequency (GHz)	2.0	2.7	2.17 – 2.69	1.0 – 2.2	1.7 – 2.0	2.0
Insertion Loss (dB)	0.37	0.17	0.22 – 0.29	0.35 – 0.50	0.22 – 0.29	0.16
Return Loss (dB)	26	20	18 – 20	20	19 – 22	24
Isolation (dB)	38.0	33.0	31.0 – 37.0	30.0 – 34.0	30.0 – 32.0	47.1
2nd / 3rd Harmonic (dBm)	–	−74.0 / −76.0 (@ f_0 = 2.7 GHz, P_{in} = 24 dBm)	−79.0 / −58.0 (@ f_0 = 2.4 GHz, P_{in} = 24 dBm)	–	−82.5 / −92.5 (@ f_0 = 1.95 GHz, P_{in} = 24 dBm)	−88.7 / −78.9 (@ f_0 = 2.0 GHz, P_{in} = 25 dBm)
Turn-on Switching Time (μs)*	0.14 (@ f_t= –)	0.15 (@ f_t= –)	0.16 (@ f_t= –)	1.7 (@ f_t= –)	4.00 (@ f_t = 300 MHz)	0.35 (@ f_t = 2.0 GHz)
Turn-off Switching Time (μs)#	–	–	–	1.24 (@ f_t= –)	–	0.32 (@ f_t = 2.0 GHz)
Total gate width of Series Tr. (mm)	–	3.9	–	–	–	3.5
Number of stacks	8	6	–	–	–	8
Supply Voltage (V)	2.5	1.8	1.65 – 3.6	2.3 – 4.8	1.8 – 3.6	2.5
Power handling capability (dBm) at P_{in}	35.0	32.0	30.0	38.5	38.0	39.5

f_t = RF frequency for the switching time measurement, f_0 = Fundamental RF frequency
*Time duration between the 50 % of the Vcontrol and the 90 % of the maximum RF peak value
#Time duration between the 50 % of the Vcontrol and the 10 % of the maximum RF peak value

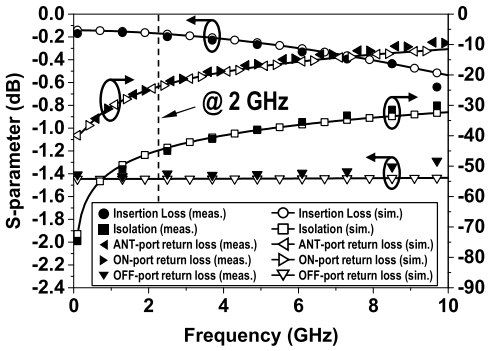

FIGURE 8. Simulation and measurement of the insertion loss, isolation, antenna-port return loss, ON-port return loss, and OFF-port return loss.

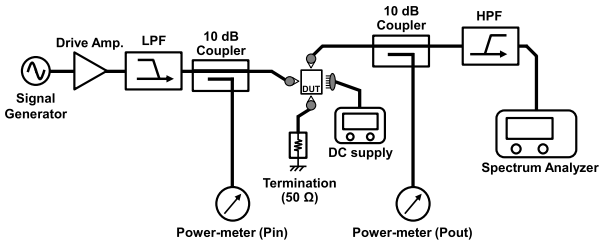

FIGURE 9. Measurement setup of the harmonic level and power handling capability.

results were de-embedded by an open-short pattern of the PCB. As shown in Fig. 8, the measurement results of the proposed SPDT switch were 0.16 dB of the insertion loss, 47.1 dB of the isolation. Antenna-port return loss, ON-port return loss and OFF-port return loss were 24.0 dB, 24.2 dB, and 1.4 dB respectively.

C. POWER HANDLING CAPABILITY AND HARMONICS

The harmonic level and power handling capability of the SPDT switch were measured by the spectrum analyzer (Keysight CXA-N9000A). The measurement setup of the harmonic level and power handling capability are shown in Fig. 9. The fundamental signal (2 GHz) was generated by the signal generator (Keysight N5182A). To apply the fundamental large signal to SPDT switch, the fundamental signal was amplified by gain-amplifier (RFHIC RWP15080-10). To decrease the 2nd and 3rd harmonic signals generated by the gain-amplifier, a low pass filter (Microwave Circuits L2G04G81) was added after gain-amplifier. For the monitoring of the input and output fundamental signal power, the coupler (Krytar 158010) and power-meter (Keysight E4417A) are used. A high pass filter (Mini-circuits VHF-2700A+) was used to lower the output signal power to a low level that the spectrum analyzer (Keysight CXA-N9000A) can endure. The input power calibration was performed to measure in real-time the input power. And the output calibration was performed to confirm the switch path ON-state and OFF-state operation. To compensate the harmonic level, the loss of output due to high pass filter was measured and the harmonic results are compensated for that loss.

The proposed switch achieved an input power handling capability of 39.5 dBm. The proposed SPDT switches exhibited 2nd harmonic level of −88.7 dBm, and 3rd harmonic level of −78.9 dBm at an input power of 25 dBm at 2 GHz.

D. PERFORMANCE COMPARISON

As shown in Table 3, the measurement results of the proposed SPDT switch are summarized and compared to state-of-the-art SPDT switches. References with faster switching

times than this work have lower power handling capabilities [2], [3], [10]. If these references increase the number of stacked transistors to improve the power handling capability, not only increase the insertion loss, but also slow down the switching time correspondingly. Other references that have similar high-power handling capability have very slow switching times like 1.7 μs and 4 μs [9], [11]. And if these references lower the value of the biasing resistors to reduce the switching time, the insertion loss increases too. Therefore, we have proposed the SPDT switch with BRBC to achieve high-power handling capability, fast switching time, low insertion loss and low 2nd harmonic level.

IV. CONCLUSION

To verify fast switching time with the BRBC, the proposed SPDT switch was fabricated and measured. The proposed SPDT switch achieved a switching time of 0.35 μs at 2 GHz. The insertion loss, isolation, and return loss at 2 GHz were 0.16 dB, 47.1 dB, and 24 dB respectively. The 2nd and 3rd harmonic levels at 25 dBm input power at 2 GHz were −88.7 dBm and −78.9 dBm, respectively. Power handling capability was 39.5 dBm input power at 2 GHz. In a further work, the BRBC will be applied to high order switches such as SP4T and SP8T in order to generally verify its usefulness.

REFERENCES

[1] E. Lahetkangas, K. Pajukoski, J. Vihriala, G. Berardinelli, M. Lauridsen, E. Tiirola, and P. Mogensen, "Achieving low latency and energy consumption by 5G TDD mode optimization," in *Proc. IEEE Int. Conf. Commun. Workshops (ICC)*, Jun. 2014, pp. 1–6.
[2] I.-Y. Lee and D. Im, "Low-power SOI CMOS antenna switch driver circuit with RF leakage suppression and fast switching time," *Electron. Lett.*, vol. 53, no. 5, pp. 293–294, Mar. 2017.
[3] B. S. Rikan, D. Kim, K.-D. Choi, A. Hejazi, J.-M. Yoo, Y. Pu, S. Kim, H. Huh, Y. Jung, and K.-Y. Lee, "T/R RF switch with 150 ns switching time and over 100 dBc IMD for wideband mobile applications in thick oxide SOI process," *Sensors*, vol. 22, no. 2, p. 507, Jan. 2022.
[4] D. Im and K. Lee, "Characterization and optimization of partially depleted SOI MOSFETs for high power RF switch applications," *Solid-State Electron.*, vol. 90, pp. 94–98, Dec. 2013.
[5] M. B. Shifrin, P. J. Katzin, and Y. Ayasli, "Monolithic FET structures for high-power control component applications," *IEEE Trans. Microw. Theory Techn.*, vol. 37, no. 12, pp. 2134–2141, Dec. 1989.
[6] D. Im, B.-K. Kim, D.-K. Im, and K. Lee, "A stacked-FET linear SOI CMOS cellular antenna switch with an extremely low-power biasing strategy," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 6, pp. 1964–1977, Jun. 2015.
[7] V. N. K. Malladi and M. Miller, "A 48 dBm peak power RF switch in SOI process for 5G mMIMO applications," in *Proc. IEEE 19th Top. Meeting Silicon Monolithic Integr. Circuits RF Syst. (SiRF)*, Orlando, FL, USA, Jan. 2019, pp. 1–3.
[8] A. Tombak, M. S. Carroll, D. C. Kerr, J.-B. Pierres, and E. Spears, "Design of high-order switches for multimode applications on a silicon-on-insulator technology," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 10, pp. 3639–3649, Oct. 2013.
[9] *High Linearity, High Power RF Switch BGS12PN10*, Infineon, Neubiberg, Germany, Aug. 2016.
[10] *BGS12WN6 Wide Band SPDT Diversity Switch With Fast Switching Speed*, Infineon, Neubiberg, Germany, Dec. 2021.
[11] *SKY13330-397LF: 0.1 to 6.0 GHz SPDT Switch*, Skyworks, Irvine, CA, USA, Mar. 2020.
[12] *SKY13278-313LF: 100 MHz to 2.5 GHz GaAs SPDT Switch*, Skyworks, Irvine, CA, USA, Aug. 2017.
[13] *PE42423: UltraCMOS SPDT RF Switch 100 MHz–6 GHz*, Peregrine Semiconductor, San Diego, CA, USA, 2019.

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