High Hole Mobility and Low Leakage Thin-Body (In)GaSb p-MOSFETs Grown on High-Bandgap AlGaSb

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ABSTRACT In this study, we demonstrated low leakage current and high mobility thin body (In)GaSb p-FETs. Through the optimization of the V/III ratio during the epitaxial growth, we achieved a highly insulating bottom $Al_{0.95}Ga_{0.05}Sb$ barrier, which eliminates the junction leakage. We also suppressed the interface trap-assisted surface leakage current by introducing $In_{0.53}Ga_{0.47}As$ surface passivation on the GaSb channel. Furthermore, GaSb/InGaSb/GaSb quantum well (QW) channel structure provided significant improvement in effective mobility (μ_{eff}) characteristics. As a result, the fabricated devices showed the lowest off-leakage current (I_{off}), subthreshold slope (S.S.) and high μ_{eff} among reported GaSb p-MOSFETs.

INDEX TERMS GaSb, III-V, ultra-thin-body (UTB), InGaAs passivation.

I. INTRODUCTION

III-V compound semiconductors have been studied as alternative channel materials for next-generation logic [1]–[5]. Inherent physical properties such as superior transport characteristics motivated the use of these materials. Recently, its low process temperature turned out as the additional benefits of III-V for monolithic 3D (M3D) integration, which is another knob to reduce the power consumption and increase the performance of complementary metal-oxide-semiconductor (CMOS) circuits [6]–[9]. However, unbalanced performance between n-FET and p-FET is one of the fundamental problems to fabricate CMOS circuits due to the relatively low hole mobility of III-V materials [5].

Among a tremendous number of material combinations of III-V compound semiconductors, III-antimonide (Sb) materials have high hole mobility exceeding 1000 cm^2/V·s, which is 5 times higher than that of Si. Moreover, the hole mobility

of III-Sb materials can be noticeably increased by strain engineering [10]–[14].

Although the potential of these materials has been reported by many groups, the progress of III-Sb FETs has been quite slow and the number of reports is limited due to the difficult material growth and material control during the device fabrication process [10]–[22]. Moreover, MOS interface control has been difficult, resulting in lower effective mobility (μ_{eff}) and high off-state leakage current (I_{off}). Indeed, the typical I_{off} of reported GaSb p-MOSFET is large even for long channel devices. Such high I_{off} includes junction leakage current and surface leakage current through a large number of interface traps at the MOS interface.

To solve these issues, in this study, we demonstrate the thin-body (In)GaSb p-MOSFET using a novel barrier underneath the channel, good MOS interface, and compressively strained InGaSb channel. First, we developed the semi-insulating the $Al_{0.95}Ga_{0.05}Sb$ (AlGaSb) barrier
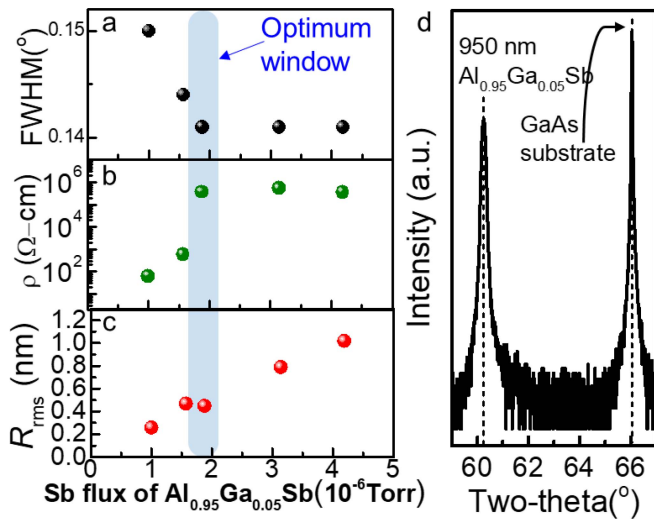
FIGURE 1. V/III ratio dependence of $Al_{0.95}Ga_{0.05}Sb$ buffer characteristics (FWHM, ρ, and R_{rms}) grown on GaAs substrate and its XRD spectra.

on a GaAs substrate to eliminate the junction leakage. Second, to form a good MOS interface and reduce interface trap-assisted surface leakage, we introduced the $In_{0.53}Ga_{0.47}As$ passivation layer on (In)GaSb channel layers. Here, we chose $In_{0.53}Ga_{0.47}As$ because $In_{0.53}Ga_{0.47}As$ has a proper band offset to confine hole at the high-quality epitaxial interface between $In_{0.53}Ga_{0.47}As$ and (In)GaSb. Moreover, good interfacial quality is expected by utilizing lower interface trap density (D_{it}) at mid-gap to valence band in $Al_2O_3/In_{0.53}Ga_{0.47}As$ compared to lattice-matched InAs passivation, which has been much studied to passivate GaSb [23], [24]. Finally, we introduced a compressively strained $In_{0.25}Ga_{0.75}Sb$ quantum well (QW) channel to enhance mobility through reduced effective mass and Coulomb scattering/thickness-fluctuation scattering [25], [26]. Through these engineering, we demonstrated high-performance (In)GaSb p-FETs showing remarkably low I_{off}, subthreshold slope (*S.S.*), and high μ_{eff}.

II. DEVICE FABRICATION

To obtain good insulating properties of the barrier layer, we grew high-quality epitaxial films of $Al_{0.95}Ga_{0.05}Sb$ using a molecule beam epitaxy (MBE). First, we carefully investigated the influence of the V/III ratio during the epitaxial growth since this parameter is very important to guarantee the insulating properties and smooth surface of the $Al_{0.95}Ga_{0.05}Sb$ buffer layer [4]. Fig. 1 summarizes the impact of Sb flux (V/III ratio) during the growth on crystal quality, electrical properties, and morphology characteristics of $Al_{0.95}Ga_{0.05}Sb$ layers. We found that there is an optimum V/III ratio considering the trade-off among full width at half maximum (FWHM) of X-ray diffraction (XRD) spectra, resistivity (ρ), and surface root mean square roughness (R_{rms}) of $Al_{0.95}Ga_{0.05}Sb$ layer. The Sb flux of 1.9×10^{-6} Torr was the balanced condition to provide high quality and good surface morphology of $Al_{0.95}Ga_{0.05}Sb$
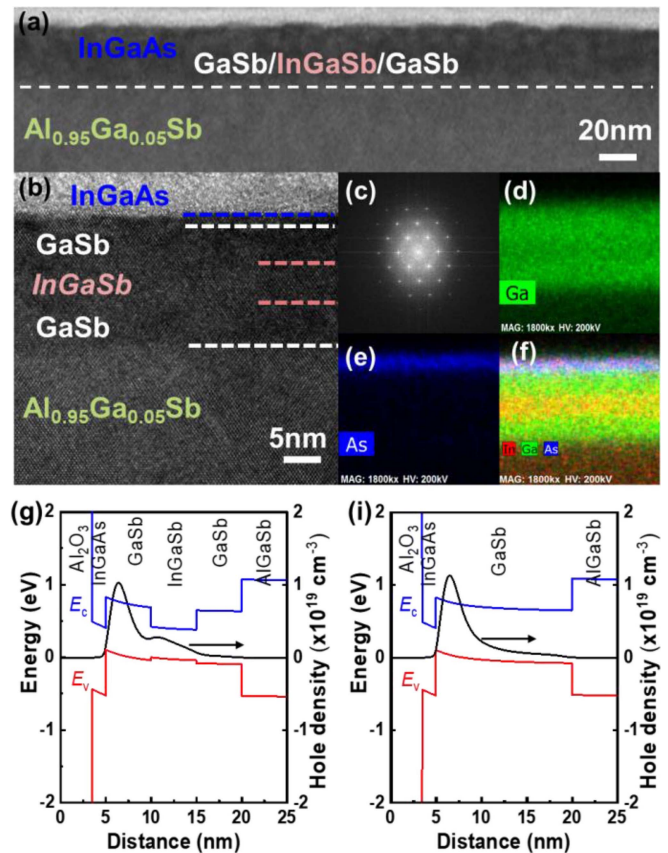

FIGURE 2. (a) Cross-sectional TEM image of the fabricated thin-body InGaAs/GaSb/InGaSb/GaSb on AlGaSb barrier on GaAs and (b) high-resolution image of (a), (c) FFT pattern of channel region, and EDX mapping image of (d) Ga (e) As (f) In, Ga, As. (g) Band diagram and carrier distribution in this sample and (i) GaSb channel sample.

film. With that growth condition, $Al_{0.95}Ga_{0.05}Sb$ shows a small FWHM of 0.14° in XRD shown in Fig. 1(b), high ρ of 0.3 MΩ·cm, and smooth surface with a low R_{rms} of 0.4 nm. We used this condition to grow the epitaxial structure for $In_{0.25}Ga_{0.75}Sb$ p-MOSFETs. For the device layers, we grew 1.5-nm-thick $In_{0.53}Ga_{0.47}As$/5-nm-thick GaSb/5-nm-thick $In_{0.25}Ga_{0.75}Sb$/5-nm-thick GaSb/950-nm-thick $Al_{0.95}Ga_{0.05}Sb$ on (100) S.I. GaAs substrates by MBE. For GaSb single-channel MOSFETs, 15-nm-thick GaSb was grown instead of 5-nm-thick GaSb/5-nm-thick $In_{0.25}Ga_{0.75}Sb$/5-nm-thick GaSb QW.

To investigate the quality of the epitaxial films, we carried out cross-sectional transmission electron microscopy (TEM) measurement. Figs. 2(a) and 2(b) show the cross-sectional TEM of the sample including GaSb/$In_{0.25}Ga_{0.75}Sb$/GaSb QW channel, indicating the excellent crystal quality of the channel layer and the abrupt interfaces between each material. Fig. 2(c)-(f) shows the Fast Fourier transform (FFT) image of the channel region and Energy-dispersive X-ray spectroscopy (EDX) mapping image of In, Ga, and As. It also confirmed single-crystalline behaviors and abrupt material interfaces. The thin InGaAs passivation layer was uniformly formed on top of the channel.
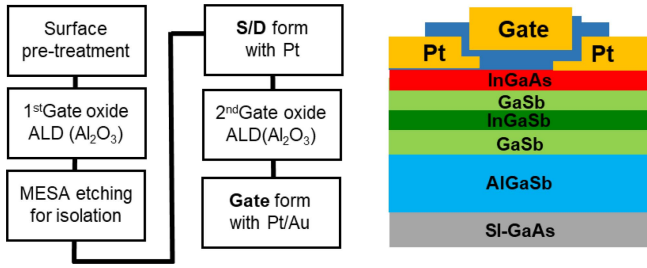
FIGURE 3. Fabrication process flow of $In_{0.25}Ga_{0.75}Sb$ QW p-MOSFET and the schematic image of the final device stricture.

FIGURE 4. Transfer curve of GaSb p-MOSFETs w/ and w/o InGaAs passivation. InGaAs reduces I_{off} and enhances I_{on}.

FIGURE 5. (a) $I_{DS} - V_{GS}$ curves of GaSb p-MOSFET with InGaAs passivation, RTA at 250°C, $L_G = 5$ μm, $W_G = 20$ μm showing low *S.S.* of 198 mV/dec and large I_{on}/I_{off} of $>10^3$ and (b) output characteristics of the device.

To see the impact of this channel structure on the carrier distribution, we calculated the band diagram and carrier distribution by solving 1D Poisson's equations. Fig. 2(g), (i) shows the band diagram and carrier distribution in InGaAs/GaSb/InGaSb/GaSb/AlGaSb and InGaAs/GaSb/AlGaSb sample. A large valence band offset between InGaAs and GaSb provides strong hole confinement in the channel layer. QW channel structure provides a higher hole population in the InGaSb layer.

Using this wafer, we fabricated $In_{0.25}Ga_{0.75}Sb$ QW and GaSb p-MOSFETs. Fig. 3 shows the device fabrication process and its schematic image of the final device cross-section.

First, we carried out the pre-treatment for the sample in HF 1% solutions for 1 min. After the pretreatment process, we deposited 5-nm-thick Al_2O_3 as the gate oxide at 250 °C by atomic layer deposition (ALD). Then, each device was isolated by mesa etching using wet etchants of BOE, Citric acid: $H_2O_2 = 3$: 1, and HCl: H_2O: $H_2O_2 = 50$: 50: 1 for Al_2O_3, InGaAs, and (In)GaSb, respectively. For source and drain ohmic contacts, we deposited 30-nm-thick Pt as a metal S/D [27], [28]. Finally, second gate oxide 10-nm-thick Al_2O_3 was deposited at 250°C by ALD and Pt gate was formed, followed by rapid thermal annealing (RTA) in the N_2 atmosphere. Here, the second gate oxide was deposited to avoid the gate leakage through the overlap region between S/D metal and gate metal, thereby, the total oxide thickness was 15 nm.

III. RESULTS AND DISCUSSION
A. IMPACT OF INGAAS PASSIVATION LAYER AND THERMAL TREATMENT IN GASB P-MOSFET
To investigate the impact of InGaAs passivation, we compared the transfer curves of the GaSb p-MOSFET with and without InGaAs passivation. The transfer characteristics of those devices are shown in Fig. 4(a). InGaAs-passivated GaSb p-MOSFET shows significant improvement in switching characteristics. On-current (I_{on}), I_{off}, and *S.S.* characteristics were improved by the InGaAs passivation, as shown in Fig. 4(b). These results strongly suggest that poor GaSb surface can be improved by thin InGaAs epitaxial passivation, resulting in higher I_{on} and reduced trap-assisted leakage and *S.S.*
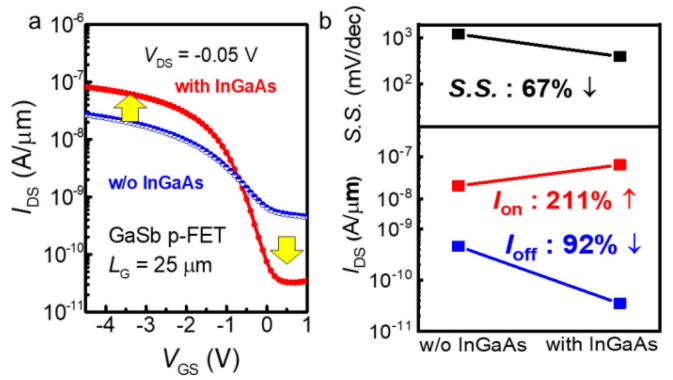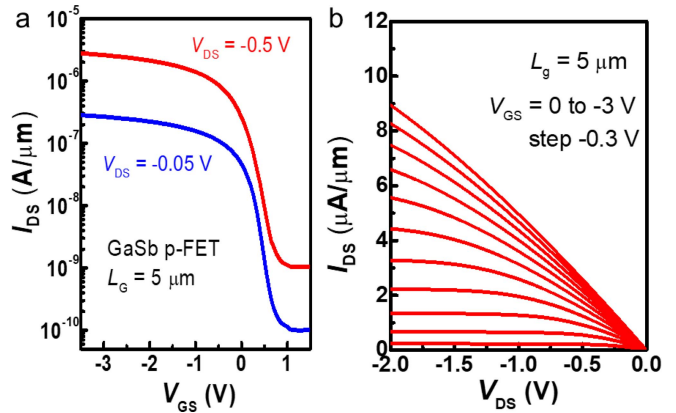
Fig. 5 shows excellent drain current (I_{DS})-gate voltage (V_{GS}) and I_{DS}-drain voltage (V_{DS}) curves of the GaSb p-MOSFET with InGaAs passivation, RTA at 250°C, gate length (L_G) = 5 μm, gate width (W_G) = 20 μm, showing small *S.S.* of 198 mV/dec, high I_{on}/I_{off} ratio of 2.3×10^3, and clear current saturation in output curve.

Since thermal treatment has been known to improve interfacial characteristics of the Al_2O_3/InGaAs interface, we carried out RTA for GaSb p-MOSFETs with InGaAs passivation [29]. Fig. 6 shows the systematic investigation of the impact of RTA temperature on switching characteristics of the devices. Here, RTA was carried out in N_2 ambient for 1 min.

In these results, the performance metrics (I_{off}, *S.S.*, I_{on}/I_{off}, μ_{eff}) improve with an increase of the annealing temperature at a relatively low-temperature range, indicating that the interfacial properties of the Al_2O_3/InGaAs passivation layer were improved by RTA. However, off-state behavior (I_{off}, *S.S.*, I_{on}/I_{off}) degrades with RTA at higher than 300°C, whereas μ_{eff} constantly increases with increasing RTA temperature up to at least 310°C. These results indicate that the degradation of off-state characteristics is probably originated
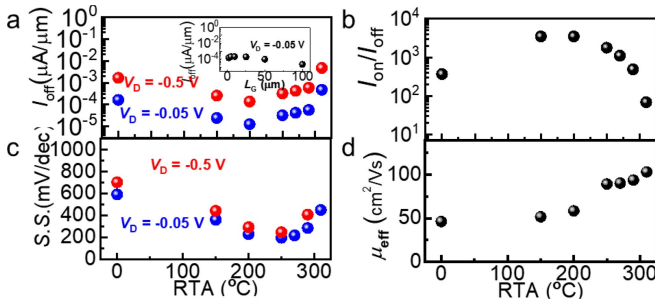
FIGURE 6. RTA temperature dependence of (a) I_{off}, (b) I_{on}/I_{off}, (c) *S.S.*, and (d) μ_{eff} characteristics of GaSb p-MOSFET with InGaAs passivation. Good off-characteristics were obtained with RTA at around 250°C, whereas μ_{eff} gradually increases with increasing RTA temperature. This indicates process modification will provide further improvement.

from junction degradation rather than D_{it} increase at the interface. Therefore, further improvement will be expected by process modification considering the trade-off between the improvement in interfacial properties and junction characteristics. In the present study, to achieve the balanced on- and off-state characteristics, we used RTA at 250°C in other devices.

B. ELECTRICAL CHARACTERISTICS OF THIN-BODY INGASB P-MOSFETS

To achieve higher mobility, we introduced the QW channel structure composed of GaSb/InGaSb/GaSb layers [25], [26]. Figures 7(a) and (b) show the $I_{DS} - V_{GS}$ and $I_{DS} - V_{DS}$ characteristics of the thin-body-GaSb/InGaSb/GaSb QW p-MOSFET with InGaAs surface passivation. Even with the lattice-mismatched InGaSb channel layer, a small I_{off} was obtained. A positive threshold voltage shift was observed due to the InGaSb layer compared to the pure GaSb channel. Output curve in Fig. 7(b) also showed a clear current saturation.

As described earlier, we introduced a QW channel structure to further enhance μ_{eff}. To see the impact of the channel structure, we plotted the on-resistance as a function of the channel length in Fig. 8(a). In this figure, the slope in InGaSb QW p-MOSFET is much smaller than that of GaSb p-MOSFET, indicating that the μ_{eff} of InGaSb QW channel is higher than that of the GaSb channel. Fig.8 (b) shows μ_{eff} characteristics in InGaSb QW p-MOSFET and GaSb p-MOSFETs. Here, we have extracted the μ_{eff} from the relationship, $\mu_{eff} = L_G \cdot I_{DS}/(W_G \cdot C_{ox} \cdot (V_{GS} - V_{th}))$, where C_{ox} and V_{th} are oxide capacitance and threshold voltage, respectively. The sheet charge density (N_s) was approximated by $C_{ox} \cdot (V_{GS} - V_{th})$. C_{ox} was estimated by measuring the C_{ox} of Pt/Al$_2$O$_3$/InGaAs control capacitor, thereby, InGaAs capacitance has not been taken account in the MOSFETs. This can slightly underestimate the μ_{eff}, but the impact should be less than 4%. The μ_{eff} in InGaSb QW p-MOSFETs showed a higher value than that of GaSb p-MOSFETs at the whole N_s range with approximately 1.7 times enhancement factor. This would be attributed to the higher mobility of the
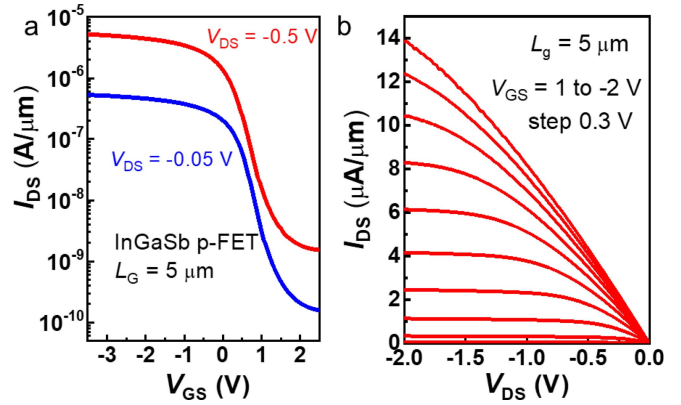

FIGURE 7. (a) $I_{DS} - V_{GS}$ curves of the GaSb/InGaSb/GaSb QW p-FET with InGaAs passivation, $L_G = 5 \mu$m, and (b) output characteristics of the device. I_{on} was significantly improved from Fig. 5, while I_{off} remaining similar.
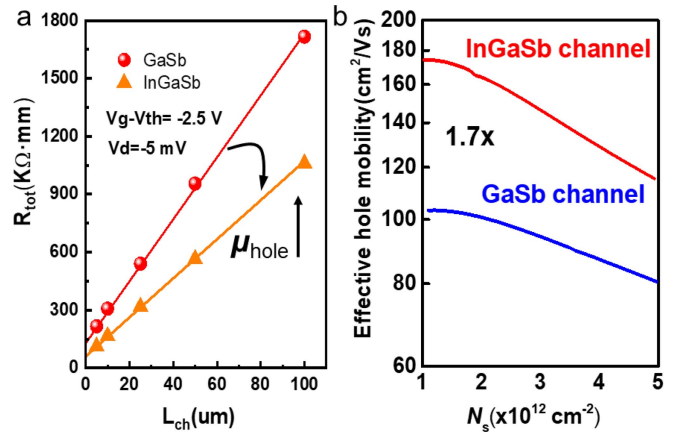

FIGURE 8. $\mu_{eff} - N_s$ characteristics of the GaSb and InGaSb QW p-FETs showing large enhancement of μ_{eff} in QW.

InGaSb channel than pure GaSb channel, whereas holes are not fully confined in the InGaSb layer. A higher hole population in the InGaSb layer successfully increased the μ_{eff} without significant change in the electrostatic performance.

C. EVALUATION OF INTERFACE AND CHANNEL QUALITY

Since off-state characteristics can degrade *S.S.* (not only by D_{it}) in Fig. 6, D_{it} extraction from *S.S.* value may not always provide correct D_{it}. Therefore, to eliminate the effect of I_{off} and extract reliable D_{it} in our devices, we investigated the temperature dependence of *S.S* in Fig. 9. We theoretically calculated *S.S.* value using the following equation and plotted them for D_{it} of 10^{11}, 10^{12}, and 10^{13} eV^{-1}·cm^{-2} in the same graph.

$$S.S. = 2.3 \frac{kT}{q}[1 + \frac{C_d + C_{it}}{C_i}] \qquad (1)$$

where k is Boltzmann's constant, q is the electronic charge, T is measurement temperature, and C_d, C_{it}, and C_i are the depletion capacitance, interface capacitance, and gate oxide capacitance respectively. Here, C_d was calculated by $k\varepsilon_0/t$,
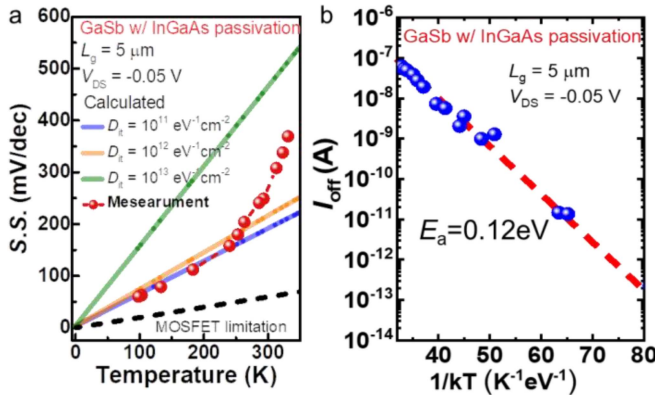
FIGURE 9. Temperature dependence of *S.S.* of GaSb p-MOSFET with InGaAs passivation. The calculated line and measured data indicate very low D_{it} in our device. Temperature dependence of I_{off} of GaSb p-MOSFET with InGaAs passivation showing not so high activation energy.

FIGURE 10. (a) $I_{DS} - V_{GS}$ curves of GaSb p-MOSFET with various W_G from 20 to 400 μm. (b) I_{off} (I_{DS} at $V_{GS} = 2.5$V) values as a function of $1/W_G$.

FIGURE 11. Benchmarks of (a) $I_{off} - V_{DS}$, (b) $\mu_{eff} - I_{on}/I_{off}$ in GaSb, and InGaSb QW p-MOSFETs.

where k, ε_0, and t are relative permittivity, vacuum dielectric constant, and channel thickness, respectively because the 15-nm-thick channel should be fully depleted. At a higher temperature than 250K, *S.S.* shows the sharp increase with increasing temperature, indicating that I_{off} degrades *S.S.* and it hinders extracting the correct *S.S.* decided by D_{it}. On the other hand, the experiment *S.S.* follows the calculated *S.S.* with D_{it} of 10^{11} eV^{-1}·cm^{-2} at low temperature, because I_{off} does not impact anymore due to sufficiently lowered I_{off} at low temperature. It should be noted that obtained D_{it} is exceptionally low for GaSb-based MOSFETs, indicating that the MOS interface is significantly improved by InGaAs passivation. Furthermore, *S.S.* is expected to be further improved by scaling EOT and further reducing D_{it}. With this very low D_{it}, μ_{eff} characteristics of the MOSFETs seems to be not sufficiently high. We think that this would be related to the channel quality and thickness. With the same gate stack, we obtained much higher mobility in InGaSb MOSFETs than GaSb MOSFETs, indicating gate stack is not a limiting factor for effective mobility in our devices. Therefore, there are many rooms to improve effective mobility by further optimization in epitaxial growth and channel structure. A potential technological issue for InGaAs passivation would be the scaling limit due to the existence of InGaAs, which will reduce the gate capacitance. However, the dielectric constant of InGaAs is 13.8, which corresponds to the EOT of 4.2 Å when the thickness is 1.5 nm Therefore, the EOT penalty will be not that large considering the possibility to further reduce the thickness by the process optimization.

To qualify the S/D junction and limiting factor of I_{off}, we extracted activation energy (E_a) of I_{off}, as in Fig. 9(b). Extracted E_a was found to be lower than half of the bandgap of GaSb channel, indicating I_{off} is still affected by trap-assisted transport and/or surface leakage at present devices. E_a extracted from InGaSb p-MOSFETs was found to be 0.13 eV, which is quite similar to the E_a of GaSb p-MOSFETs. Improvement in crystal quality and process
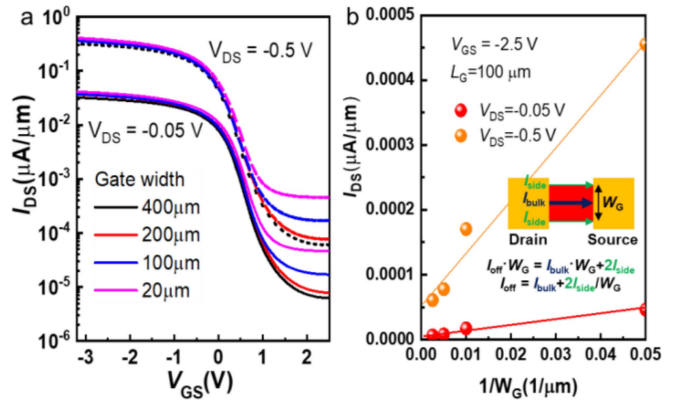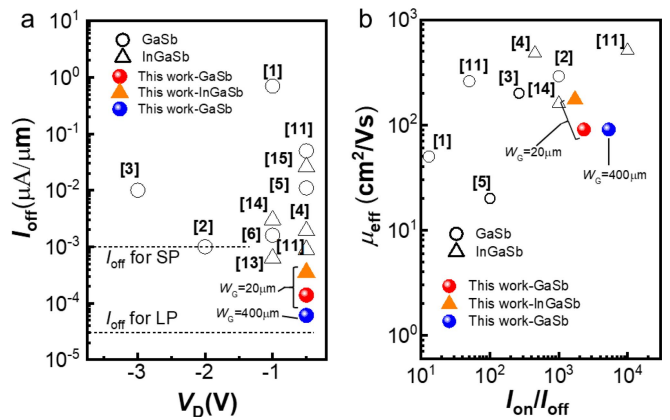
optimization will provide further improvement in the device performance.

To investigate the amount of surface leakage current more quantitively, we evaluated the impact of the mask layout on I_{off}. We compared the electrical characteristics of GaSb p-MOSFETs with various W_G from 20 to 400 μm. Fig. 10(a) shows the transfer curves of GaSb p-MOSFETs with various W_G. I_{on} and *S.S.* characteristics were almost the same, but I_{off} improves with increasing W_G, indicating there is still noticeable surface leakage on the sidewall in the present devices. Fig. 10(b) shows the I_{off} as a function of $1/W_G$. Here, I_{off} is taken at $V_{GS} = 2.5$V. We found that dots pointed in this graph shows a linear relationship indicating leakage portion flowing through the sidewall (I_{side}), where is not covered by InGaAs. Here, we extracted the bulky component of I_{off} (I_{bulk}), which is proportional to W_G, and I_{side} from the y-intercept and slope of the graph. I_{bulk}/I_{side} at V_{DS} of -0.05V and -0.5V was found to be 5.45×10^{-6} μA/μm/4.12×10^{-4} μA/μm^2, 5.40×10^{-5} μA/μm/4.06×10^{-3} μA/μm^2, respectively. These results strongly indicate that I_{side} due to non-passivated surfaces by InGaAs should be reduced to achieve lower I_{off} in the future.

Fig. 11 shows the benchmark of $I_{off} - V_{DS}$, and $\mu_{eff} - I_{on}/I_{off}$ in GaSb and InGaSb p-MOSFETs reported so far [1-15]. For a fair comparison, we took all I_{off} from long channel devices. We found that our thin-body (In)GaSb p-FETs with InGaAs passivation shows remarkable off-state characteristics as well as on-state characteristics.

IV. CONCLUSION

In this work, we investigated thin-body (In)GaSb p-MOSFETs with bulk, channel, and interface engineering. First, we systematically investigated the buffer layer quality of $Al_{0.95}Ga_{0.05}Sb$ with various Sb effective fluxes to guarantee low substrate leakage with high electrical resistance. We obtained a high-quality buffer layer of $Al_{0.95}Ga_{0.05}Sb$ with FWHM of $0.14°$, ρ of 0.3 MΩ·cm, and smooth surface with R_{rms} of 0.4 nm at Sb effective flux of 1.9×10^{-6} Torr. Using this condition, we grew the epitaxial structure for (In)GaSb pFETs. Second, to improve hole mobility, we used channel strain and reducing coulomb scattering with GaSb/InGaSb/GaSb QW channel structure. Third, in interface engineering, we demonstrated the InGaAs passivation layer for low surface leakage with low D_{it} value.

Using this high-quality new thin-body-(In)GaSb epi-structure, we fabricated with the gate-oxide-first process and analyzed the electrical characteristics. We measured the transfer curve of with and without InGaAs passivation layer GaSb p-MOSFETs and indicating that with InGaAs passivation layer sample shows better switching performance of I_{on}/I_{off} and S.S. than without the InGaAs passivation layer. Then, we analyzed electrical characteristics with different RTA temperature. The data show that device performance was improved with increasing RTA temperature under $300\,°C$, however higher than $300°C$, the off-state behavior (I_{off}, S.S., I_{on}/I_{off}) is degraded. To achieve the balanced on- and off-state characteristics, we used RTA at $250°C$. Our (In)GaSb pFETs show the excellent electrical properties of low I_{off}, S.S., and high μ_{eff} via optimization of the insulating barrier, improved interface quality with InGaAs passivation layer and QW channel structure. These devices showed nearly record-performance in $I_{off} - V_D$ and $\mu_{eff} - I_{on}/I_{off}$ among reported (In)GaSb based devices.

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