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A 4410-ppi Resolution Pixel Circuit for High Luminance Uniformity of OLEDoS Microdisplays

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ABSTRACT This paper proposes a pixel circuit with high resolution and high luminance uniformity for organic light emitting diode-on-silicon (OLEDoS) microdisplays. The proposed pixel circuit employs a simple structure that consists of four n-channel MOSFETs and one capacitor, resulting in high resolution. In addition, this circuit compensates for the threshold voltage (V_{th}) variation of the driving transistor caused by the body effect, which increases the V_{th} as the source-to-body voltage of the driving transistor increases, thus reducing the emission current deviation, resulting in a high luminance uniformity. Moreover, the proposed pixel circuit extends the data voltage range using the capacitive coupling of the storage capacitance and the parasitic capacitance at the gate node of the driving transistor to precisely control the emission current. To verify the performance of the proposed pixel circuit, a test pattern with an array of the proposed 4T1C pixel circuits was fabricated on a single-crystalline silicon wafer as a backplane using a 110 nm standard CMOS process with 5.5 V high-voltage devices. The proposed pixel circuit occupies a unit sub-pixel area of 5.76μm × 1.92μm, which corresponds to a resolution of 4410 pixels per inch. The measurement results show that the emission current deviation error of the proposed pixel circuit ranges between −1.16% and +1.14%, which is improved from between −45.97% to +45.42% achieved in the conventional current-source type 2T1C pixel circuit, which does not compensate for the V_{th} variation of the driving transistor. Moreover, the measured data voltage range of the proposed pixel circuit is extended to 1.618 V, which is 8.17 times wider than that of the conventional pixel circuit. Therefore, the proposed pixel circuit is very suitable for high resolution and high luminance uniformity of OLEDoS microdisplays.

INDEX TERMS OLED, OLED-on-silicon, OLEDoS, microdisplay, high resolution, high luminance uniformity, pixel circuit.

I. INTRODUCTION

Recently, microdisplays have been increasingly adopted for augmented reality (AR) and virtual reality (VR) applications such as head-mounted displays, head-up displays, and hologram projectors. Especially, organic light-emitting diode (OLED)-on-silicon (OLEDoS) microdisplays have been more widely used for AR and VR applications than other microdisplays with liquid crystal-on-silicon or digital micro-mirror device because of their many advantages, including high contrast ratio, fast optical response time, and excellent color reproducibility [1]–[7].

To realize high quality AR and VR applications, the OLEDoS microdisplays need to have high resolution and high luminance uniformity. For high resolution, the OLEDoS pixel circuit should have a simple structure that can be integrated into a unit sub-pixel area of tens of μm^2. However, since the size of the driving transistor in the pixel circuit decreases as the sub-pixel area decreases, the threshold voltage (V_{th}) variation of the driving transistor increases due to variation in the fabrication process, such as a variation in the dopant concentration and gate oxide capacitance from pixel to pixel [8]. Moreover, as the V_{th} variation increases, the emission current deviation increases, resulting in luminance imbalance. Therefore, it is necessary for the pixel circuit to compensate for the V_{th} variation of the driving transistor to achieve high luminance uniformity. In addition, as the

emission current of the high-efficiency OLEDs such as tandem OLEDs [9] decreases to hundreds of pico-amperes, the data voltage range of the OLEDoS pixel circuit becomes narrower, thus reducing the accuracy of the programmed data voltage of the pixel circuit, resulting in poor luminance uniformity.

To solve the aforementioned problems, several pixel circuits for OLEDoS microdisplays have been studied [10]–[15]. The current programming pixel circuits in [10], [11] compensate for the V_{th} variation of the driving transistor. However, they are not suitable for high resolution displays because they have too complex structure to be integrated into a limited sub-pixel area. In addition, it is difficult for such pixel circuits to program the emission current within a row line time at low gray levels due to the large parasitic capacitance of the data line. The voltage programming pixel circuits in [13]–[15] compensate for the V_{th} variation of the driving transistor only at a zero source-to-body voltage, and cannot compensate for the V_{th} variation caused by the body effect; this is because these circuits sample V_{th} according to a specific reference voltage.

In this paper, a voltage programming pixel circuit for high resolution and high luminance uniformity OLED microdisplays is proposed. The proposed pixel circuit employs a simple structure with four n-channel MOSFETs and one capacitor. In addition, this circuit employs a diode-connection method in [16], which programs the data voltage while sampling $V_{th,N1}$, to compensate for the V_{th} variation due to the body effect by storing V_{th} in the storage capacitor, thus reducing the emission current deviation, resulting in a high luminance uniformity. Moreover, the proposed pixel circuit extends the data voltage range using the capacitive coupling of the storage capacitance and the parasitic capacitance at the gate node of the driving transistor, and thus can precisely control the emission current. Section II describes the operational principle and mathematical analysis of the proposed pixel circuit. In Section III, the experimental results of the fabricated test pattern are analyzed and compared with previous works. Finally, the conclusions are given in Section IV.

II. PROPOSED PIXEL CIRCUIT AND OPERATION

Fig. 1(a) and (b) respectively show the schematic and timing diagram of the proposed pixel circuit, which consists of four n-channel MOSFETs and one capacitor, and operates in the reset, programming and threshold voltage sampling, and emission phases. N1 is a driving transistor that generates the emission current flowing through the OLED, which is determined by the gate-to-source voltage of N1 ($V_{GS,N1}$). N2 and N3 are the switching transistors, which are controlled by the SCAN signal. Here, N2 connects the source node of N1 to the DATA signal line, and N3 connects the gate and drain nodes of N1. N4, which is controlled by the EM signal, is a switching transistor to turn off the OLED device for a high contrast ratio. The body of all N1–N4 is biased to the ground. C_S is a storage capacitor that samples the

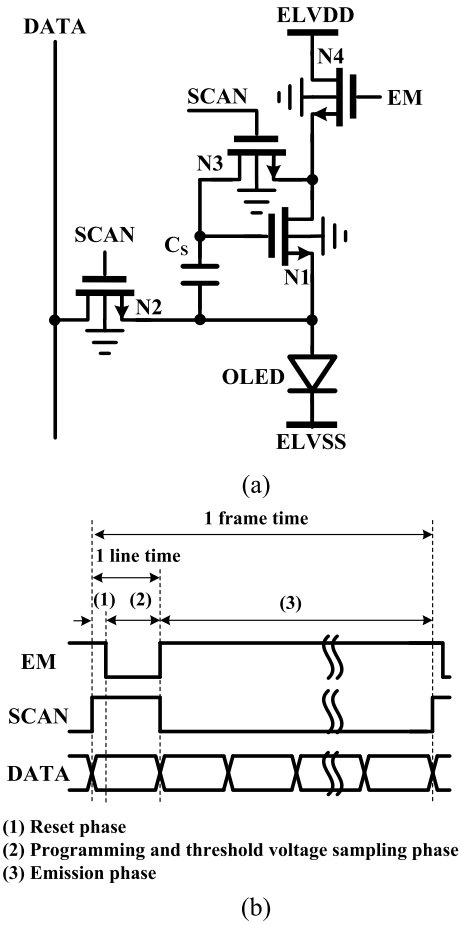

FIGURE 1. (a) Schematic and (b) timing diagram of the proposed pixel circuit.

V_{th} of the driving transistor and holds $V_{GS,N1}$ during the emission phase.

In the reset phase shown in Fig. 2(a), the SCAN signal becomes high to turn on N2 and N3, and the EM signal becomes high to turn on N4. Then, the gate and drain node voltages of N1 are reset to ELVDD, and the source node of N1 begins to program for DATA voltage (V_{DATA}). At low gray levels, since V_{DATA} is less than the turn-on voltage of the OLED, the current does not flow through the OLED. On the other hand, at high gray levels, since V_{DATA} is slightly greater than the turn-on voltage of the OLED, the current less than the target maximum emission current flows through the OLED.

In the programming and threshold voltage sampling phase shown in Fig. 2(b), the SCAN signal becomes high to turn on N2 and N3, and the EM signal becomes low to turn off N4. Then, the gate and drain nodes of N1 are connected, forming a diode-connection, and thus their voltages are discharged to $V_{DATA} + V_{th,N1}$, where $V_{th,N1}$ is the V_{th} of N1 and C_S samples $V_{th,N1}$, which can be given by

$$V_{th,N1} = V_{th0} + \gamma\left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right), \qquad (1)$$

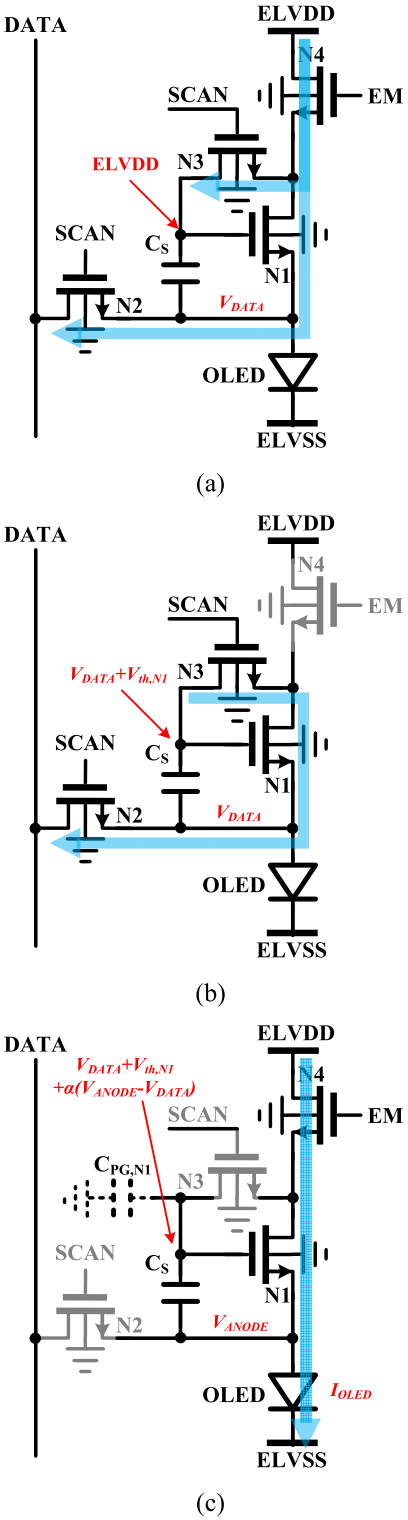

FIGURE 2. **Detailed operations of the proposed pixel circuit in the (a) reset phase, (b) programming and threshold voltage sampling phase, and (c) emission phase.**

where V_{th0}, $2\Phi_F$, V_{SB}, and γ are the threshold voltage at a zero source-to-body voltage, the surface potential, the source-to-body voltage, and a body effect coefficient, respectively [17]. In this phase, since the source node of N1 is completely programmed to V_{DATA}, and $V_{th,N1}$ is sampled considering the body effect, (1) can be expressed as

$$V_{th,N1} = V_{th0} + \gamma\left(\sqrt{|2\Phi_F + V_{DATA}|} - \sqrt{|2\Phi_F|}\right). \quad (2)$$

Here, the body is biased to the ground.

In the emission phase shown in Fig. 2(c), the SCAN signal becomes low to turn off N2 and N3, and the EM signal becomes high to turn on N4. Then, the current of N1 flowing through the OLED increases the anode voltage of the OLED from V_{DATA} to V_{ANODE}. Accordingly, the gate node voltage of N1 ($V_{G,N1}$) is changed due to the capacitive coupling of C_S and the parasitic capacitance at the gate node of N1 ($C_{PG,N1}$), and can be expressed as

$$\begin{aligned} V_{G,N1} &= V_{DATA} + V_{th,N1} + \alpha(V_{ANODE} - V_{DATA}) \\ &= (1-\alpha)V_{DATA} + \alpha V_{ANODE} + V_{th,N1}, \end{aligned} \quad (3)$$

where $\alpha = C_S/(C_S + C_{PG,N1})$. Consequently, $V_{GS,N1}$ can be expressed as

$$\begin{aligned} V_{GS,N1} &= V_{G,N1} - V_{ANODE} \\ &= (1-\alpha)(V_{DATA} - V_{ANODE}) + V_{th,N1}. \end{aligned} \quad (4)$$

The emission current flowing through the OLED (I_{OLED}) is equal to the current of N1 generated by $V_{GS,N1}$ (I_{N1}), which is less than several hundred pA within the subthreshold region over the entire gray level, and thus can be expressed as

$$\begin{aligned} I_{OLED} &= I_{N1} \\ &= I_o \exp\left(\frac{V_{GS,N1} - V_{th,N1}}{\eta V_T}\right) \\ &= I_o \exp\left\{\frac{(1-\alpha)(V_{DATA} - V_{ANODE})}{\eta V_T}\right\}, \end{aligned} \quad (5)$$

where I_0, η, and V_T are the residual drain current, subthreshold slope factor, and thermal voltage, respectively.

As shown in (5), I_{OLED} is independent of $V_{th,N1}$, indicating that the V_{th} variation is compensated. In this way, the proposed pixel circuit samples $V_{th,N1}$ in the threshold voltage sampling phase and compensates for $V_{th,N1}$ variation due to the body effect by canceling out $V_{th,N1}$. Moreover, V_{ANODE} can be expressed as

$$\begin{aligned} V_{ANODE} &= \text{ELVSS} + V_{OLED} \\ &= \text{ELVSS} + nV_T \ln\left(\frac{I_{OLED}}{I_S}\right), \end{aligned} \quad (6)$$

where, n, I_S, and V_{OLED} are the empirical constant, the reverse saturation current of the OLED, and the voltage across OLED, respectively [13]. From (5) and (6), V_{ANODE} in the emission phase can be derived as

$$V_{ANODE} = \frac{\eta\text{ELVSS} + n\eta V_T \ln\left(\frac{I_o}{I_S}\right) + n(1-\alpha)V_{DATA}}{\eta + n(1-\alpha)}. \quad (7)$$

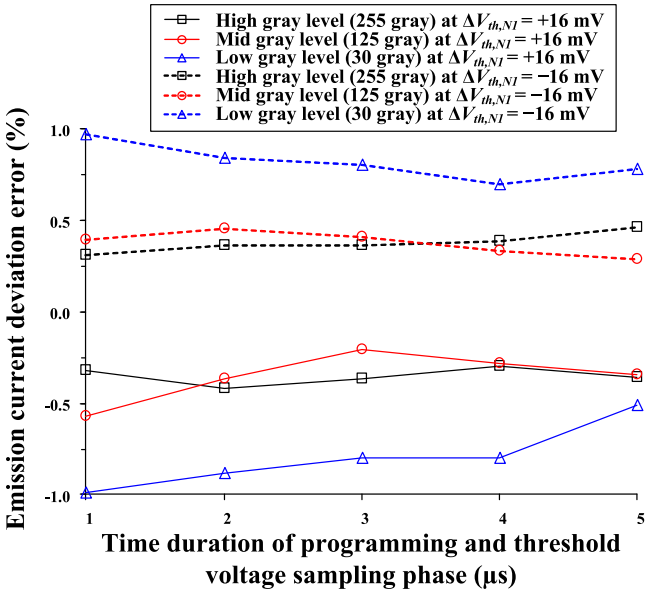

FIGURE 3. Simulated emission current deviation errors of the proposed pixel circuit for low, mid, and high gray levels according to the time duration of the programming and threshold voltage sampling phase when $V_{th,N1}$ variation is ±16 mV.

As shown in (7), V_{ANODE} is proportional to V_{DATA}. Therefore, as (V_{DATA}–V_{ANODE}) is scaled by (1 – α), as expressed in (5), the change in I_{OLED} according to V_{DATA} is suppressed, and thus the V_{DATA} range can be extended.

The time durations for the reset phase, and programming and threshold voltage sampling phase were determined to 1 μs and 4 μs, respectively. The time durations were determined considering the RC delay of the SCAN, EM, and DATA lines of the proposed pixel circuit in the target application with 0.68-in WQXGA 120 Hz. Fig. 3 shows the simulation result of the emission current deviation error of the proposed pixel circuit for the low (30 gray), mid (125 gray), and high gray (255) levels according to the time duration of the programming and threshold voltage sampling phase when $V_{th,N1}$ variation is ±16 mV. The simulation result shows that the emission current deviation error is achieved to be within 1% when the time duration is 1 μs. Therefore, the proposed pixel circuit has a good compensation ability.

III. EXPERIMENTAL RESULTS

The proposed pixel circuit was fabricated using a 110 nm standard CMOS process with 5.5 V high-voltage devices. Fig. 4(a) and (b) show the microphotograph of the fabricated test pattern of the proposed pixel circuit array and the layout of the proposed pixel circuit, respectively. Fig. 4(c) shows the detailed layout of the proposed pixel circuit revealing the layers below third metal layer. The proposed pixel circuit occupies a unit sub-pixel area of 5.76 μm × 1.92 μm, corresponding to a resolution of 4410 pixels per inch (ppi), and the storage capacitor is implemented with the metal-insulator-metal capacitor using the third and fourth layers. The detailed design parameters are summarized in Table 1.

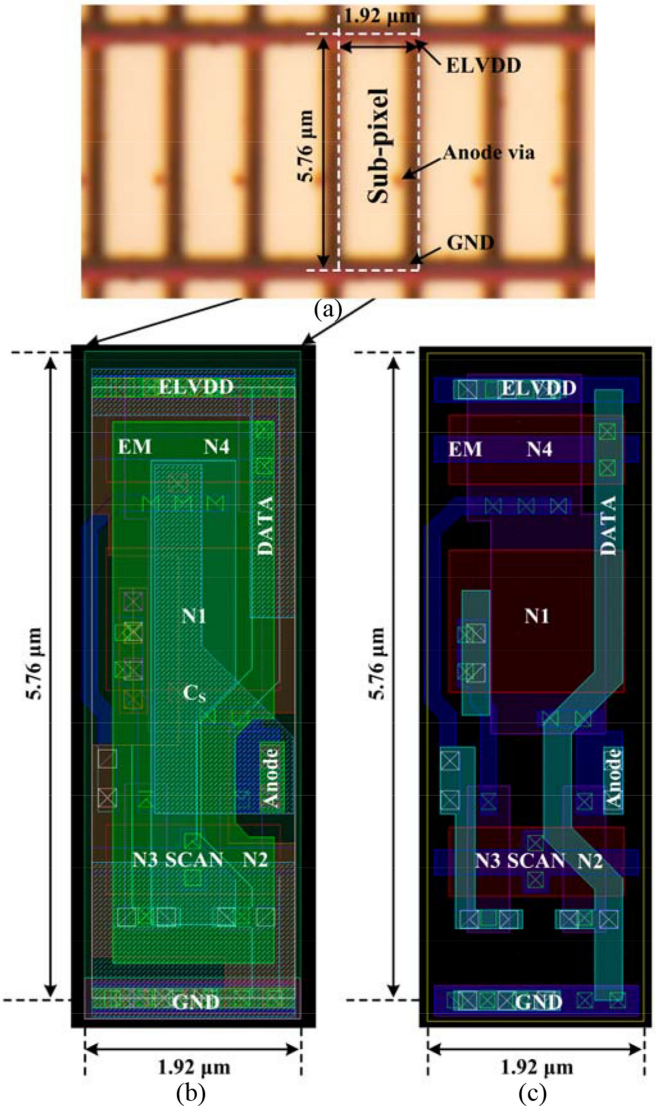

FIGURE 4. (a) Microphotograph of the fabricated test pattern of the proposed pixel circuit array, (b) layout of the proposed pixel circuit, and (c) its detailed layout showing the layers below the third metal layer.

The maximum luminance used in this work is 200 cd/m^2, which is widely used in microdisplay applications [18]. In addition, the maximum emission currents were determined using the white OLED efficiency, maximum luminance, and transmittances of the red, green, and blue color filters.

Although the test pattern of the pixel circuits was fabricated on a single crystalline silicon backplane, as the size of the driving transistor decreases, the $V_{th,N1}$ variation can increase due to variation in the fabrication process from pixel to pixel. To investigate such a $V_{th,N1}$ variation, transfer characteristics of the driving transistors were measured from 24 driving transistors in the fabricated test pattern according to the source node of N1 ($V_{S,N1}$), and then $V_{th,N1}$ was extracted. Fig. 5(a) shows the measured $V_{th,N1}$ using a maximum g_m method [19], where g_m is the transconductance of the driving transistor, showing that the measured $V_{th,N1}$

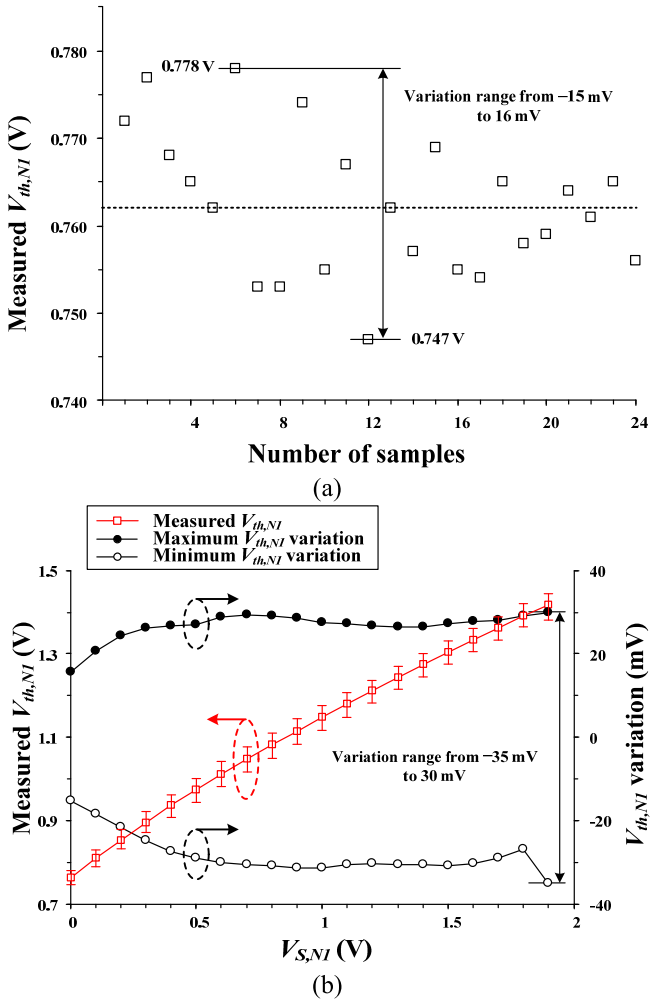

FIGURE 5. (a) Measured $V_{th,N1}$ (a) from 24 driving transistors using the maximum g_m method at a $V_{S,N1}$ of 0 V and (b) when $V_{S,N1}$ ranges from 0 V to 1.9 V.

TABLE 1. Design parameters of the proposed pixel circuit.

Design parameter	Value
Process with device	110 nm standard CMOS process with 5.5 V high-voltage device
ELVDD (V)	4
ELVSS (V)	−4
(W/L) ratio of N1 (μm/μm)	1.08/1.34
(W/L) ratio of N2 and N3 (μm/μm)	0.4/0.65
(W/L) ratio of N4 (μm/μm)	1.08/0.65
Capacitance of C_S (fF)	23.6
Color depth (bit)	8
Unit sub-pixel area (μm × μm)	5.76 × 1.92
Spatial resolution (ppi)	4410
Maximum luminance (cd/m^2)	200
White OLED efficiency (cd/A)	25
Maximum emission current (pA)	Red: 210 Green: 320 Blue: 190

variation ranges from −15 mV to 16 mV at a $V_{S,N1}$ of 0 V. Fig. 5(b) shows the measured $V_{th,N1}$, which increases from 0.762 V to 1.417 V due to the body effect as $V_{S,N1}$ increases from 0 V to 1.9 V, resulting in a $V_{th,N1}$ variation ranging from −35 mV to 30 mV. Such above $V_{th,N1}$ variations are compensated and verified through the proposed pixel circuit as follows.

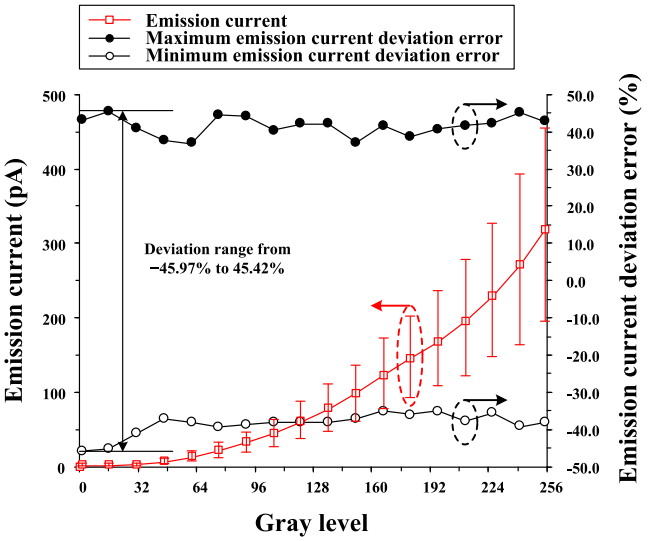

FIGURE 6. Measured emission current and its deviation error of the conventional current-source type pixel circuit using 24 samples according to 8-bit gray level.

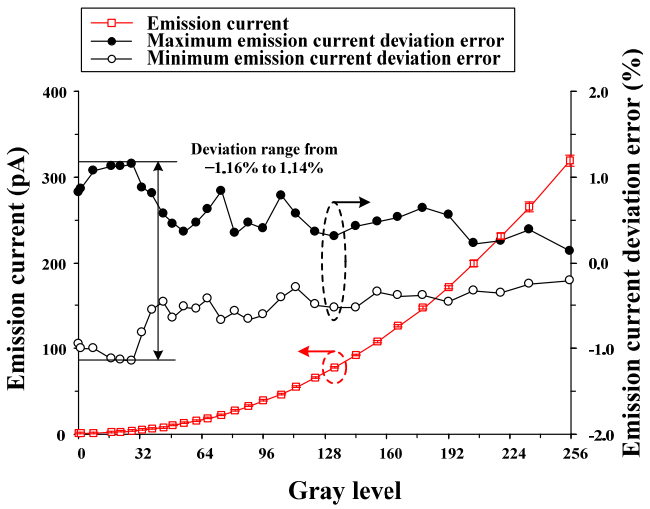

FIGURE 7. Measured emission current and its deviation error of the proposed pixel circuit using 24 samples according to 8-bit gray level.

To verify the performance of the proposed pixel circuit, the emission currents were measured from 24 pixel circuits in the fabricated test pattern at a maximum emission current of 320 pA, which corresponds to a maximum green luminance of 200 cd/m^2 at a video gamma of 2.2. Fig. 6 shows the measured emission current and its deviation error of the conventional current-source type 2T1C pixel circuit [20], which does not compensate for the V_{th} variation of the driving transistor, according to 8-bit gray level. The measurement results show that a large emission current deviation error occurs,

TABLE 2. Performance comparison of the proposed pixel circuit with previous works.

Index	[10]	[11]	[12]	[13]	This work
Process	0.35 μm CMOS process with 3.3 V device	90 nm CMOS process with 6 V device	90 nm CMOS process with 6 V device	-	110 nm CMOS process with 5.5 V device
Pixel circuit components	5T1C	3T1C	4T1C	4T2C	4T1C
Programming and driving method	Voltage programming and current driving	Voltage programming and current driving	Voltage programming and current driving	Voltage programming and current driving	Voltage programming and current driving
Unit sub-pixel area (μm × μm)	12.6 × 4.2	9 × 3	9 × 3	6.3 × 3.15	5.76 × 1.92
Spatial resolution (ppi)	2016	2822	2822	4032	4410
Emission current deviation error (%)	-	−1.86 to 1.84	−1.63 to 1.15	-	−1.16 to 1.14
V_{th} compensation	Without compensation	With compensation	With compensation	With compensation	With compensation

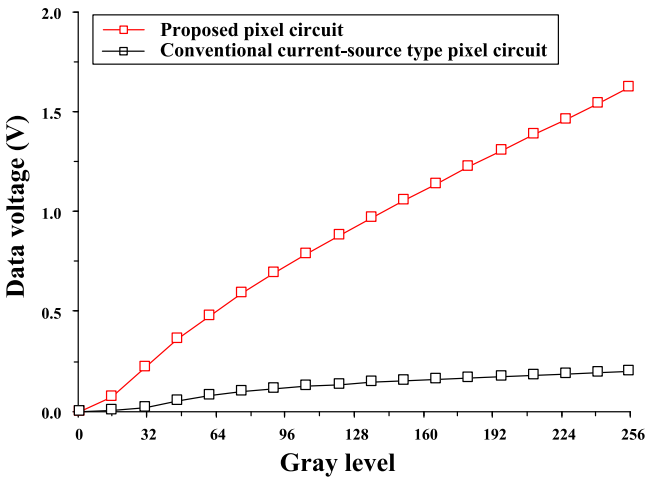

FIGURE 8. Measured data voltage ranges of the proposed pixel circuit and the conventional current source-type pixel circuit according to 8-bit gray level.

ranging from −45.97% to 45.42%, because the $V_{th,N1}$ variation is not compensated. Fig. 7 shows the measured emission current and its deviation error of the proposed pixel circuit according to 8-bit gray level. The measurement results show that the emission current deviation error decreases to between −1.16% to 1.14% because the $V_{th,N1}$ variation is compensated, demonstrating that the proposed pixel circuit can improve the luminance uniformity. Fig. 8 shows the measured data voltage ranges of the proposed pixel circuit and the conventional pixel circuit. The measured data voltage range of the proposed pixel circuit is extended to 1.618 V, which is 8.17 times wider than that of the conventional pixel circuit, which is 0.198 V, and thereby the emission current can be more precisely controlled. Table 2 shows the performance comparison of the proposed pixel circuit with previous works. Compared to these previous works, the proposed pixel circuit has the lowest emission current deviation error, thus achieving the highest luminance uniformity. In addition, the proposed pixel circuit occupies the smallest unit sub-pixel area of 5.76 μm × 1.92 μm, thus achieving a 9.4% higher spatial resolution than the state-of-the-art work in [15], which has a unit sub-pixel area of 6.3 μm × 3.15 μm.

IV. CONCLUSION

This paper proposes a pixel circuit for high resolution and high luminance uniformity of OLEDoS microdisplays. The proposed pixel circuit employs a simple structure for high resolution, which has four n-channel MOSFETs and one capacitor. In addition, this circuit compensates for the V_{th} variation of the driving transistor caused by the body effect, thus reducing the emission current deviation, resulting in high luminance uniformity. Moreover, the proposed pixel circuit extends the data voltage range using the capacitive coupling effect, and thus can precisely control the emission current. The performance of the proposed pixel circuit was verified with measurement results of the fabricated test pattern and compared with those of previous works. Compared to these previous works, the proposed pixel circuit occupies the smallest unit sub-pixel area of 5.76 μm × 1.92 μm, corresponding to a resolution of 4410 ppi. In addition, this circuit has the least emission current deviation error and thus achieves the highest luminance uniformity, while extending the data voltage range up to 1.618 V. Therefore, the proposed pixel circuit is very suitable for high resolution and high luminance uniformity of OLEDoS microdisplays.

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